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reliability designed, reliability delivered

Design for Excellence: Printed Circuit Boards (PCBs)

NCAB Presentation

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Design for Excellence for PCBs: Abstract

- Designing printed boards today is more difficult than ever before because of the increased lead free process temperature requirements and associated changes required in manufacturing.
- Not only has the density of the electronic assembly increased, but many changes are taking place throughout the entire supply chain regarding the use of hazardous materials and the requirements for recycling.
- Suppliers to the industry have had to rethink their materials and processes. Thus, everyone designing or producing electronics has been or will be affected.

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Course Outline: Design for Excellence: PCBs

- MODULE 1
  - Introduction
  - DfR & Physics of Failure (PoF)
  - Industry Standards
  - Laminate Selection
- MODULE 2
  - Plated Through Vias (PTVs)
    - How to Test/Qualify a Reliable PTV?
  - Cleanliness & Electrochemical Migration
- MODULE 3
  - Surface Finish Selection
  - Shipping, Handling, Storage
  - Supplier Selection & Auditing

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Design for Excellence Part I: Printed Circuit Boards (PCBs)

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What is DfX?

- Primary definition: Methodology that involves various groups with knowledge of different parts of the product lifecycle advising the Design Engineering functions during the design phase

- Alternative definition: Process of assessing issues *beyond the base functionality* before physical prototype
  - Base Functionality: Meeting customer expectations of function, cost, and size
  - Other Issues: Manufacturability, Reliability, Testability, Sourcing, Environment

Why These Issues Now?

- Manufacturability: Realization that quality control is not sufficient by itself to minimize defect occurrence
- Testability: Inability to rely on physical access due to increasing densities
- Sourcing: Contract manufacturing + automation + off-the-shelf
- Reliability: As electronic technology reaches maturity, there is less differentiation in price and performance with a reduction in part margins
- Environment: Legislation (REACH, RoHS, etc.) and customer awareness

Why Design for Excellence (DfX)?

- The foundation of a successful product is a robust design
  - Provides margin
  - Mitigates risk from defects
  - Satisfies the customer

Who Controls Hardware Design?

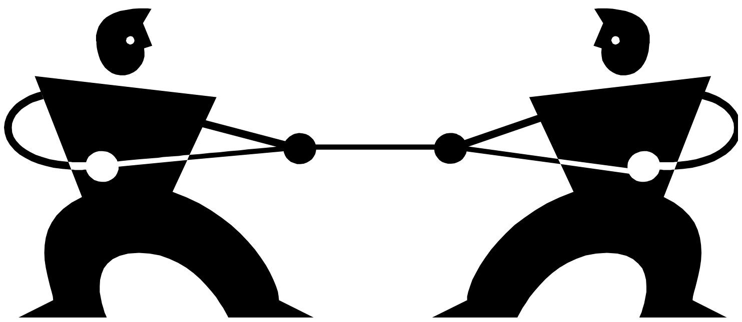
Electrical Designer

- Component selection
  - Bill of materials (BOM)
  - Approved vendor list (AVL)

Mechanical Designer

- PCB Layout
- Other aspects of electronic packaging

Both parties play a critical role in minimizing hardware mistakes during new product development



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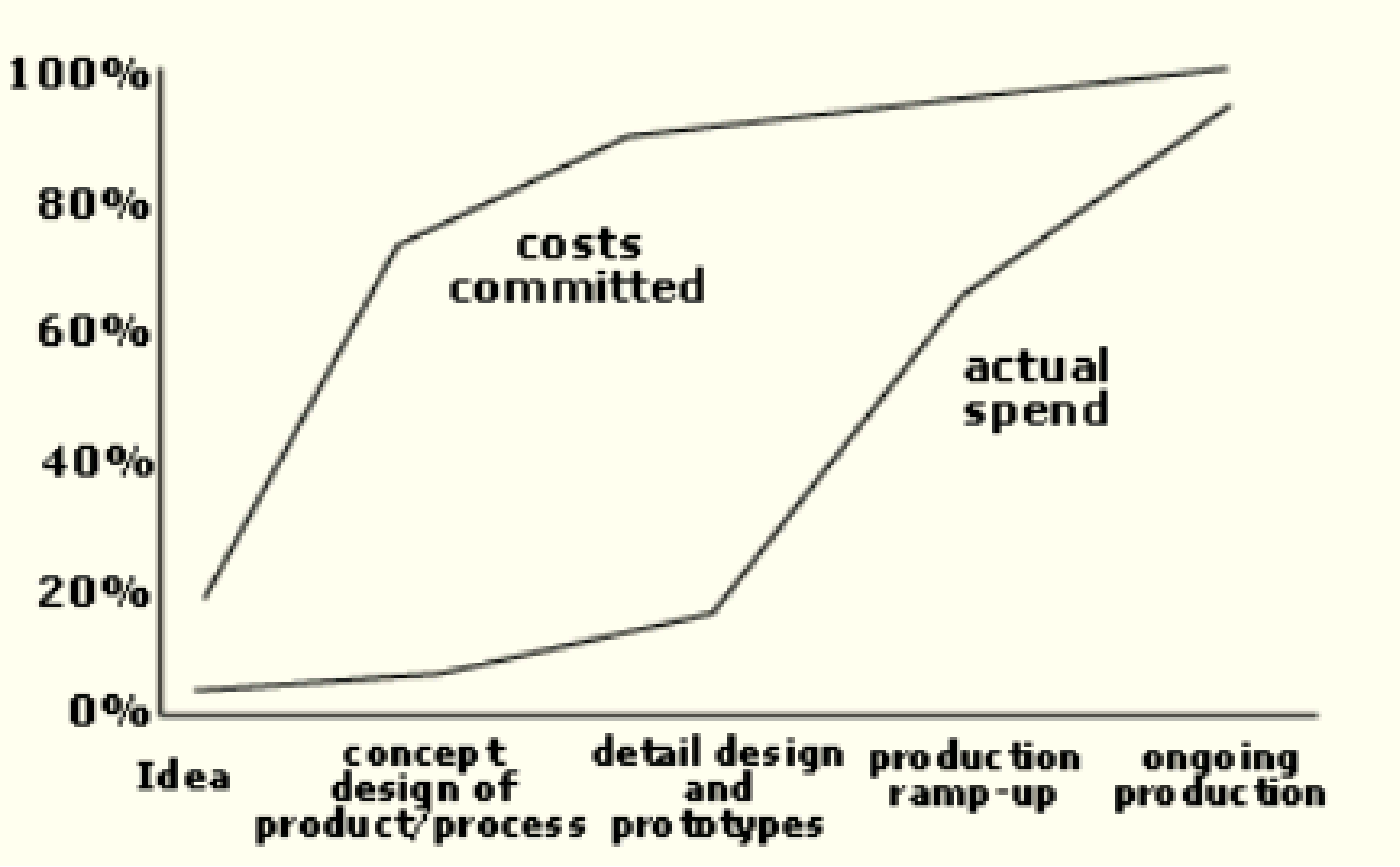
When Do Mistakes Occur?

- Insufficient exchange of information between electrical design and mechanical design
- Poor understanding of supplier limitations
- Customer expectations (reliability, lifetime, use environment) are not incorporated into the new product development (NPD) process

There can be many things that "you don't know you don't know"

Why DfX: Leverage in Product Design

http://www.ami.ac.uk/courses/topics/0248_dfx/index.html



70% of a Product's Total Cost is Committed by Design

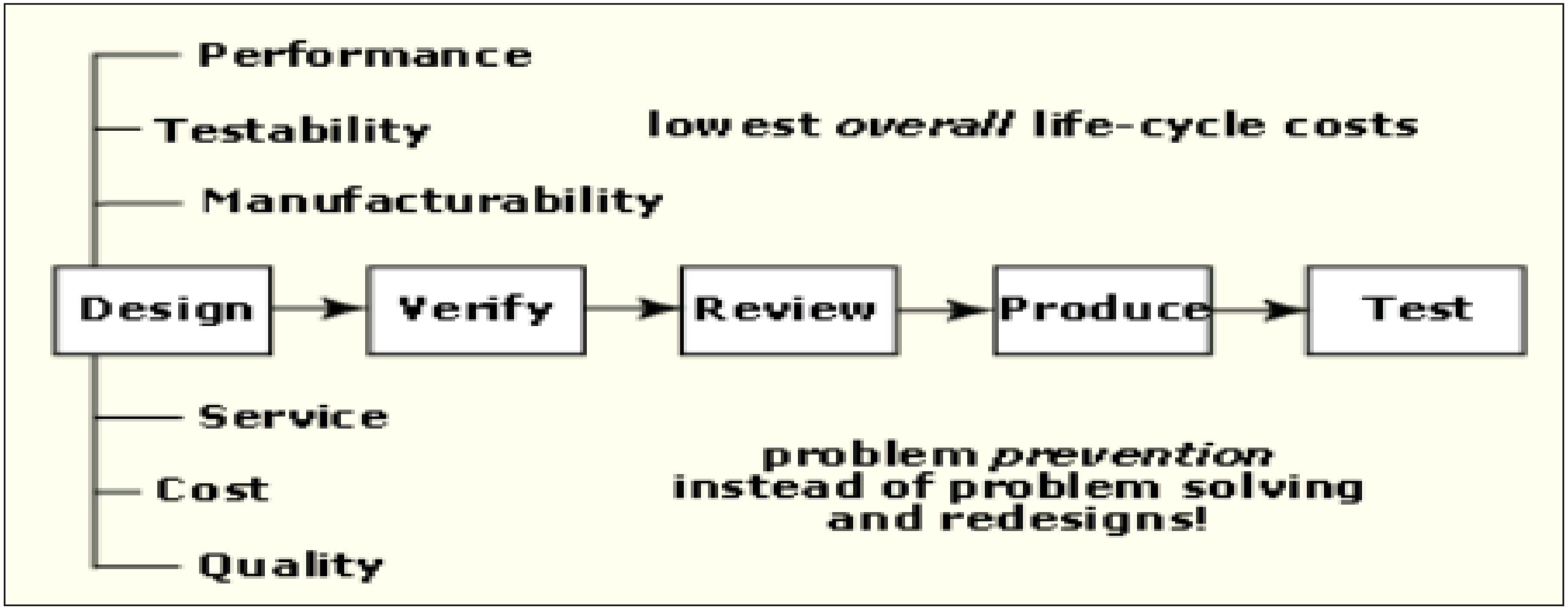
Why DfX: Faster & Cheaper

- Electronic Original Equipment Manufacturers (OEMs) that use design analysis tools
  - Hit development costs 82% more frequently
  - Average 66% fewer re-spins
  - Save up to $26,000 in re-spins

Aberdeen Group, Printed Circuit Board Design Integrity: The Key to Successful PCB Development, 2007
http://new.marketwire.com/2.0/rel.jsp?id=730231

How to DfX?

- Successful DFX efforts require the integration of product design and process planning into a cohesive, interactive activity known as Concurrent Engineering



DfX Implementation

- Many organizations have developed DfX Teams to speed implementation
  - Success is dependent upon team composition and gating functions
- <u>Challenges</u>: Classic design teams consist of electrical and mechanical engineers trained in the ‘science of success’
  - DfX requires the right elements of personnel and tools

DfX Team

- Component engineer
- Design, Electrical, Layout Engineer(s)
- Physics of failure expert (mechanical / materials)
- Manufacturing engineer
  - Box level (harness, wiring, board-to-board connections)
  - Board / Assembly
- Engineer cognizant of environmental legislation
- Testing engineer
  - Proficient in in circuit test (ICT) / Joint Test Action Group (JTAG) / functional
- Thermal engineer (depending upon power requirements)
- Reliability engineer?
  - Depends. Many classic reliability engineers provide **limited** value in the design process due to over-emphasis on statistical techniques and environmental testing

DfX Tools (Examples)

- **Manufacturability**: Valor - Mentor Graphics
- **Sourcing**: Modification of DfM, Product Lifecycle Management (PLM) tools
- **Testability**: Valor (test access), Computer Aided Manufacturing / Design (CAM CAD) Test Suite - Mentor Graphics, etc.
- **Reliability**: Finite Element Analysis (FEA), DfR Solutions Sherlock
- **Environment**: Greensoft, IHS, IPC-175X

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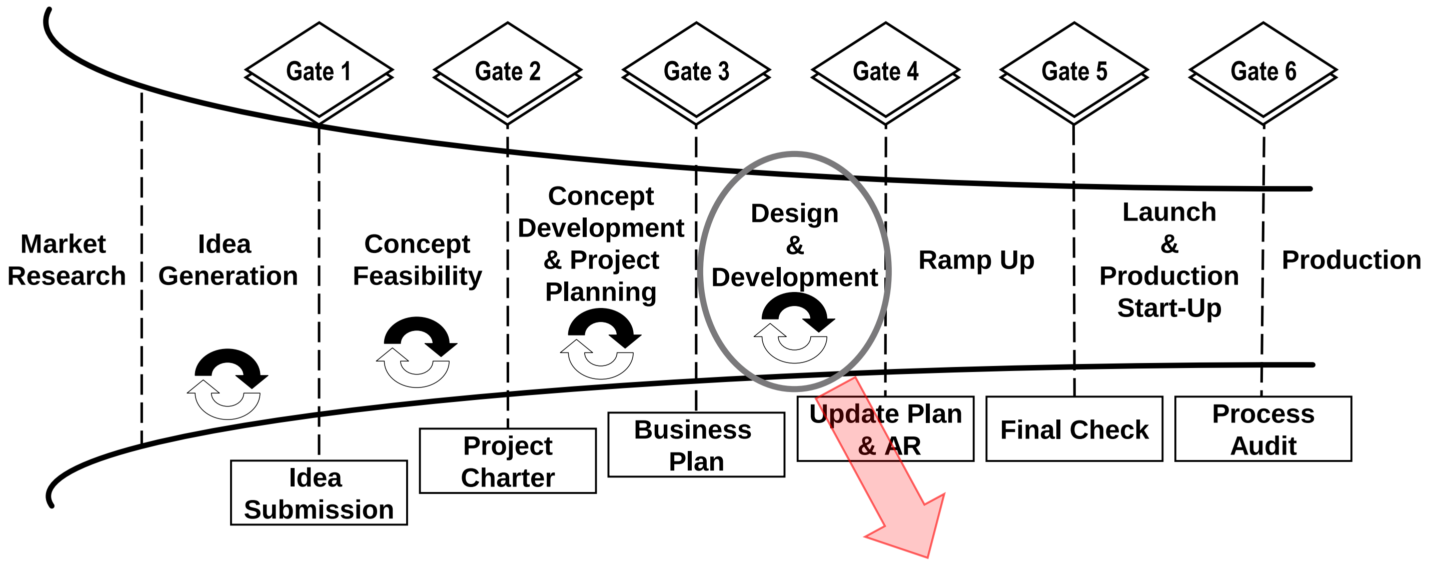
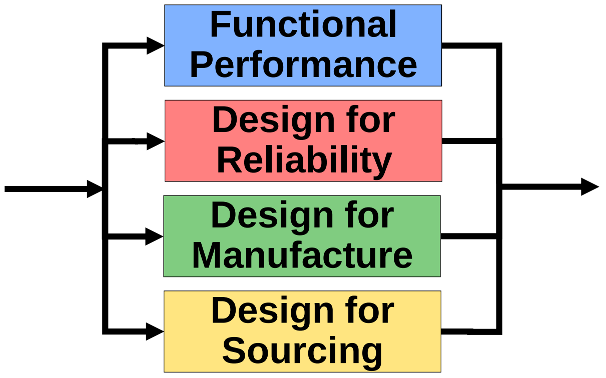
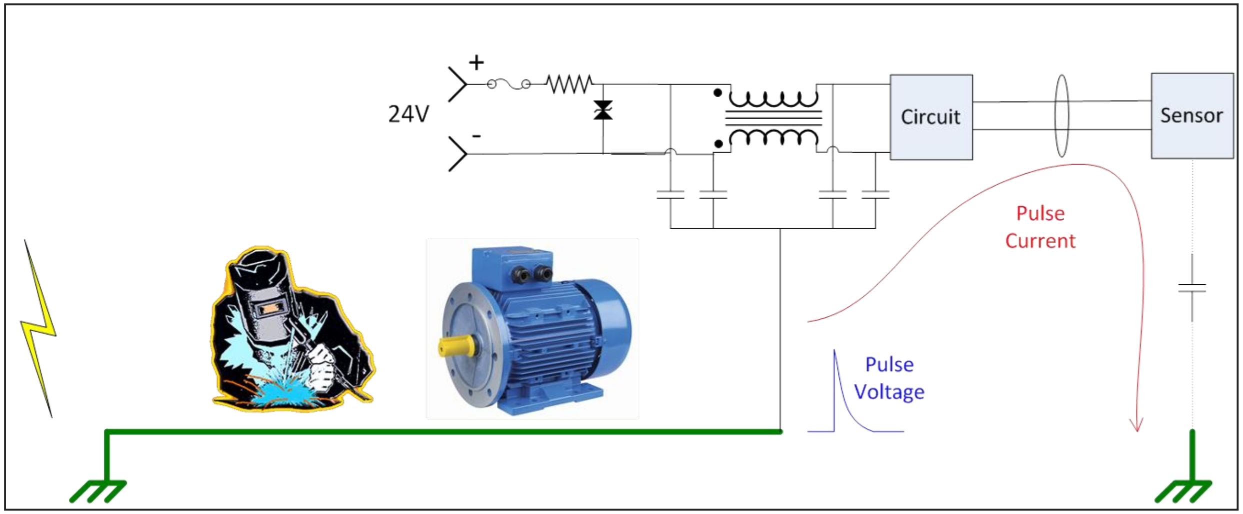
Gating DfX



- Goal: Simultaneously optimizing the design
- Reality: Need for specific gating activities (design reviews)



- Review products from *electrical, thermal, mechanical, vibration, component, manufacturability, reliability* & perspectives to give full 360° view



Example Ground Surge

The figure shows where ground surge can affect the circuit yet the product passes IEC61000-4-5 surge.

Formal design reviews & tools often overlooked

- Organization lacks special expertise
- Design organizations removed from manufacturing

Perform design reviews at all levels:

- Bare Board
- Circuit Board Assemblies
- Chassis/Housing Integration Packaging
- System Assembly

Perform design reviews with actual electronic assembly source

- Good design for one supplier & set of assembly equipment may not be good for another

Design for Reliability (DfR) Defined

- DfR: A process for ensuring the reliability of a product or system during the design stage *before* physical prototype

- Reliability: The measure of a product's ability to
  - …perform the specified function
  - …at the customer (with their use environment)
  - …over the desired lifetime

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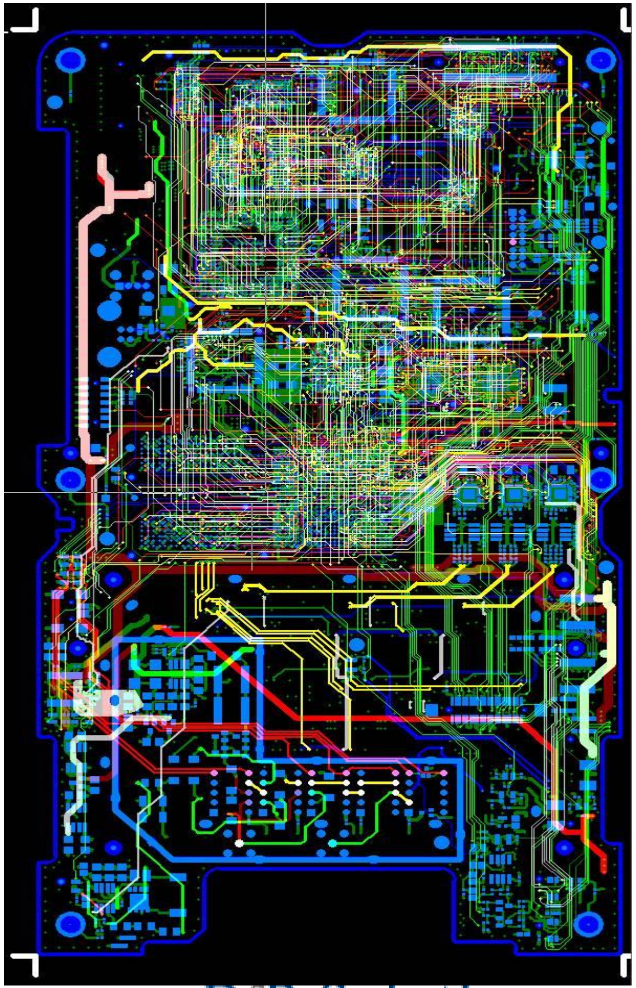
Reality of Design for Reliability (DfR)

- Ensuring reliability of electronic designs is becoming increasingly difficult
  - Increasing complexity of electronic circuits
  - Increasing power requirements
  - Introduction of new component and material technologies
  - Introduction of less robust components

- Results in multiple potential drivers for failure



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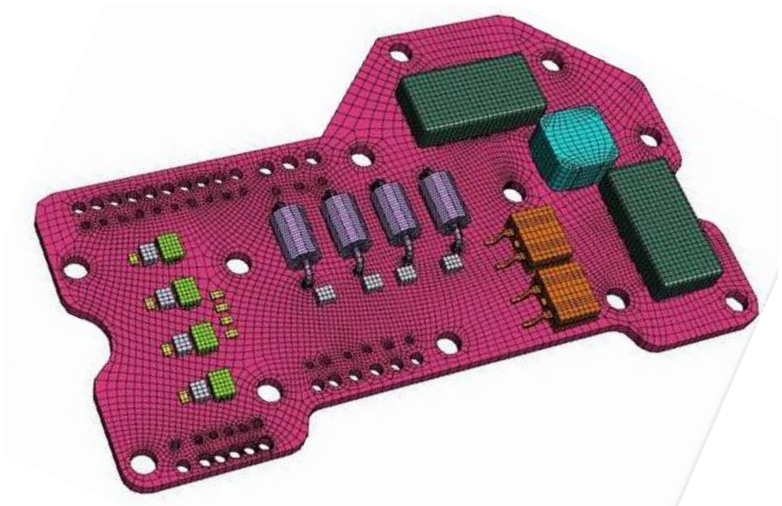
Reality (continued)

- Predicting reliability is becoming problematic
  - Standard MTBF calculations tend to be inaccurate
  - A physics-of-failure (PoF) approach can be time-intensive and not always definitive (limited insight into performance during operating life)



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Defining Reliability Goals

- Identify & document two key metrics
  - *Desired lifetime*
    - Defined as time the *customer* is satisfied with
    - Actively used in development of part and product qualification
  - *Product performance*
    - Returns during the warranty period
    - Survivability over lifetime at a set confidence level
    - MTBF or MTTF
      - Avoid unless required by customer

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Perspective on Desired Product Lifetimes

Cell Phones:	18 to 36 months
Laptop Computers:	24 to 36 months
Desktop Computers:	24 to 60 months
Medical (External):	5 to 10 years
Medical (Internal):	7 years
High-End Servers:	7 to 10 years
Industrial Controls:	7 to 15 years
Appliances:	7 to 15 years
Automotive:	10 to 15 years (warranty)
Avionics (Civil):	10 to 20 years
Avionics (Military):	10 to 30 years
Telecommunications:	10 to 30 years
Solar	25 years (warranty)

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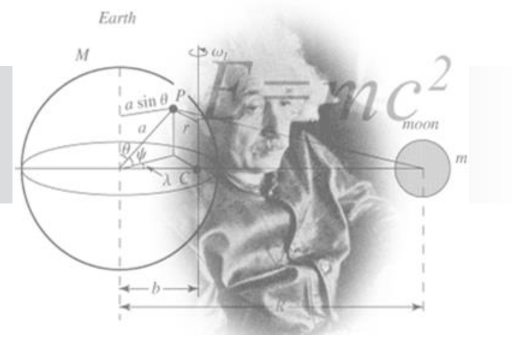
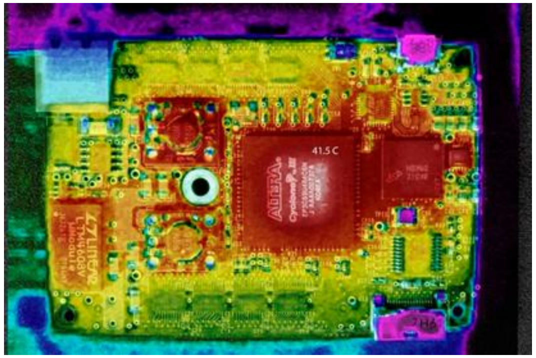
Physics of Failure (PoF)



- PoF Definition: The use of science (physics, chemistry, etc.) to capture an understanding of failure mechanisms and evaluate useful life under actual operating conditions
- Using PoF, design, perform, and interpret the results of *accelerated* life tests
  - Starting at design stage
  - Continuing throughout the lifecycle of the product
- Start with standard industry specifications
  - Modify or exceed them
  - Tailor test strategies specifically for the individual product design and materials, the use environment, and reliability needs

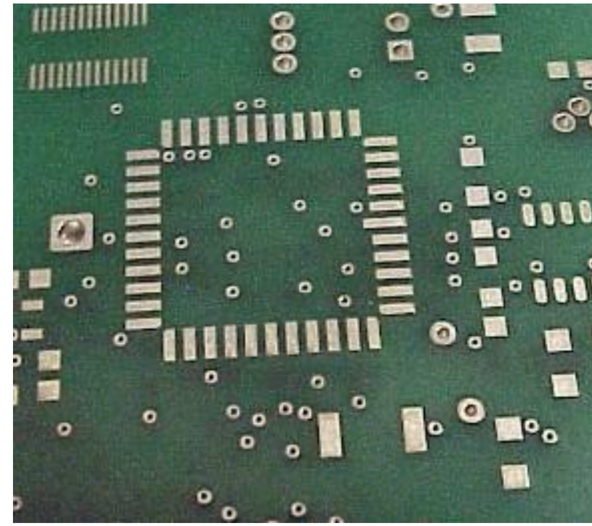
Physics of Failure Definitions

- Failure of a physical device or structure (i.e. hardware) can be attributed to the gradual or rapid degradation of the material(s) in the device in response to the stress or combination of stresses the device is exposed to, such as:
  - Thermal, Electrical, Chemical, Moisture, Vibration, Shock, Mechanical Loads . . .



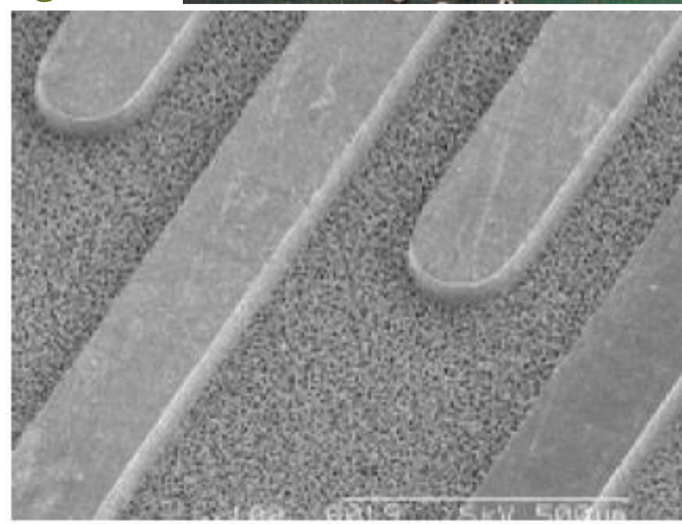
- Failures May Occur:
  - Prematurely
  - Gradually
  - Erratically

PCB PoF Example: Silver and Sulfur



- Immersion silver (ImAg) introduced in the 1990's as the 'universal finish'

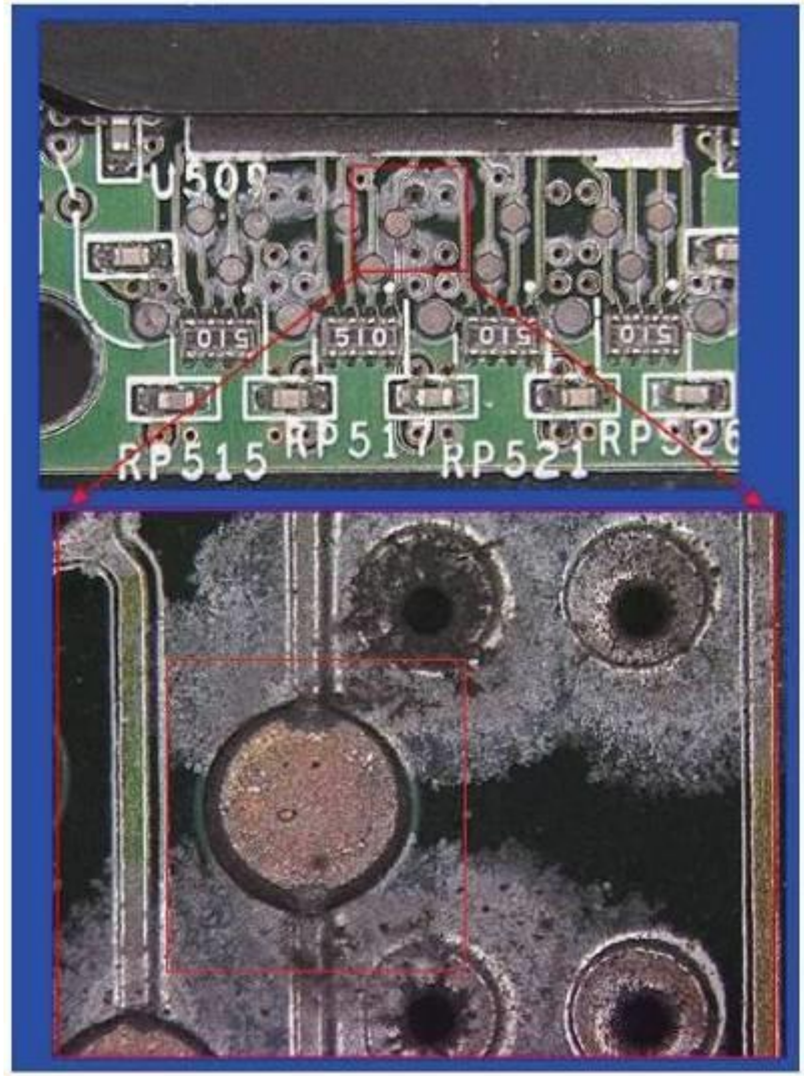
- Benefits
  - Excellent flatness, low cost, long-term storage



- Problem
  - Sulfur reacts with silver
  - Induces creeping corrosion

Immersion Silver Finish (Creeping Corrosion)

- Failures observed within months
  - Sulfur-based gases attacked exposed immersion silver
  - Non-directional migration (creeping corrosion)
- Occurred primarily in environments with high sulfur levels
  - Rubber manufacturing
  - Gasoline refineries
  - Waste treatment plants



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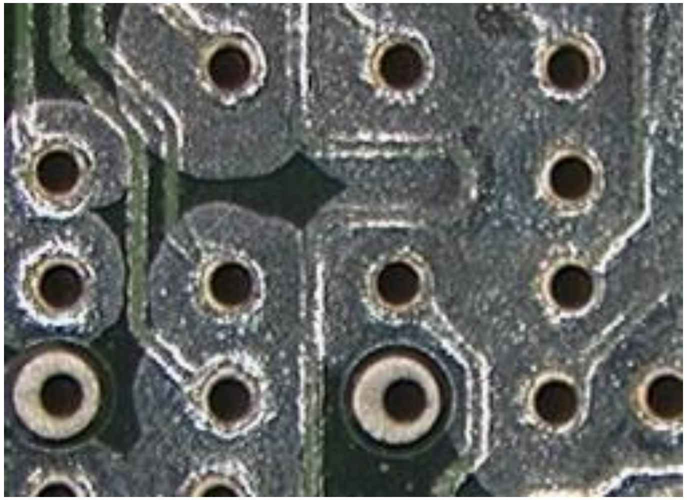
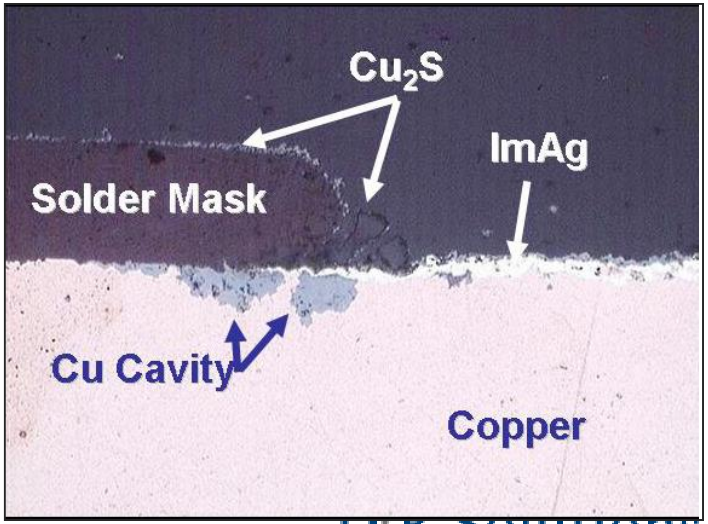
Immersion Silver Finish: Findings

- Analysis identified copper as the creeping element (not silver)
- Cross-sections identified corrosion sites near areas with no or minimal immersion silver
  - Galvanic reaction was initiating and accelerating corrosion behavior
- What went wrong?





PoF and Testing

- Failure #1
  - Test coupons were not representative of actual product
  - No solder mask defined pads, no plated through holes
- Failure #2
  - Industry test environments are limited to 70% relative humidity(RH), chamber limitations
  - Actual use environment can be more severe

Conditions	Temp (°C)	RH (%)	H_2S (ppb)	Cl_2 (ppb)	NO_2 (ppb)	SO_2 (ppb)
Indoor	30±1	70±2	10±1.5	10±1.5	200±30	100±15
Outdoor	30±1	70±2	100±15	20±3	200±30	200±30

Telcordia

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PoF and Immersion Silver

- The Final Failure?

- Acknowledging the reactivity of silver with sulfur and moving beyond ‘test to spec’ to truly capture potential risks
  - The ‘physics’ was not well enough understood before the new material was released

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Design for Reliability At Concept: Specifications

- Can DfR mistakes occur at this stage?
  - No……….and Yes
- Failure to capture and understand product specifications at this stage lays the groundwork for mistakes at schematic and layout
- Important specifications to capture at concept stage
  - Reliability expectations
  - Use environment
  - Dimensional constraints
- A perfectly designed & constructed PCB can still be unreliable if materials are chosen poorly – even if made to IPC Class 3!

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Industry Standard Design Guidelines

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New DfX Standard In Progress!

IPC-2231:Design for Excellence (DFX) Guideline During the Product Lifecycle

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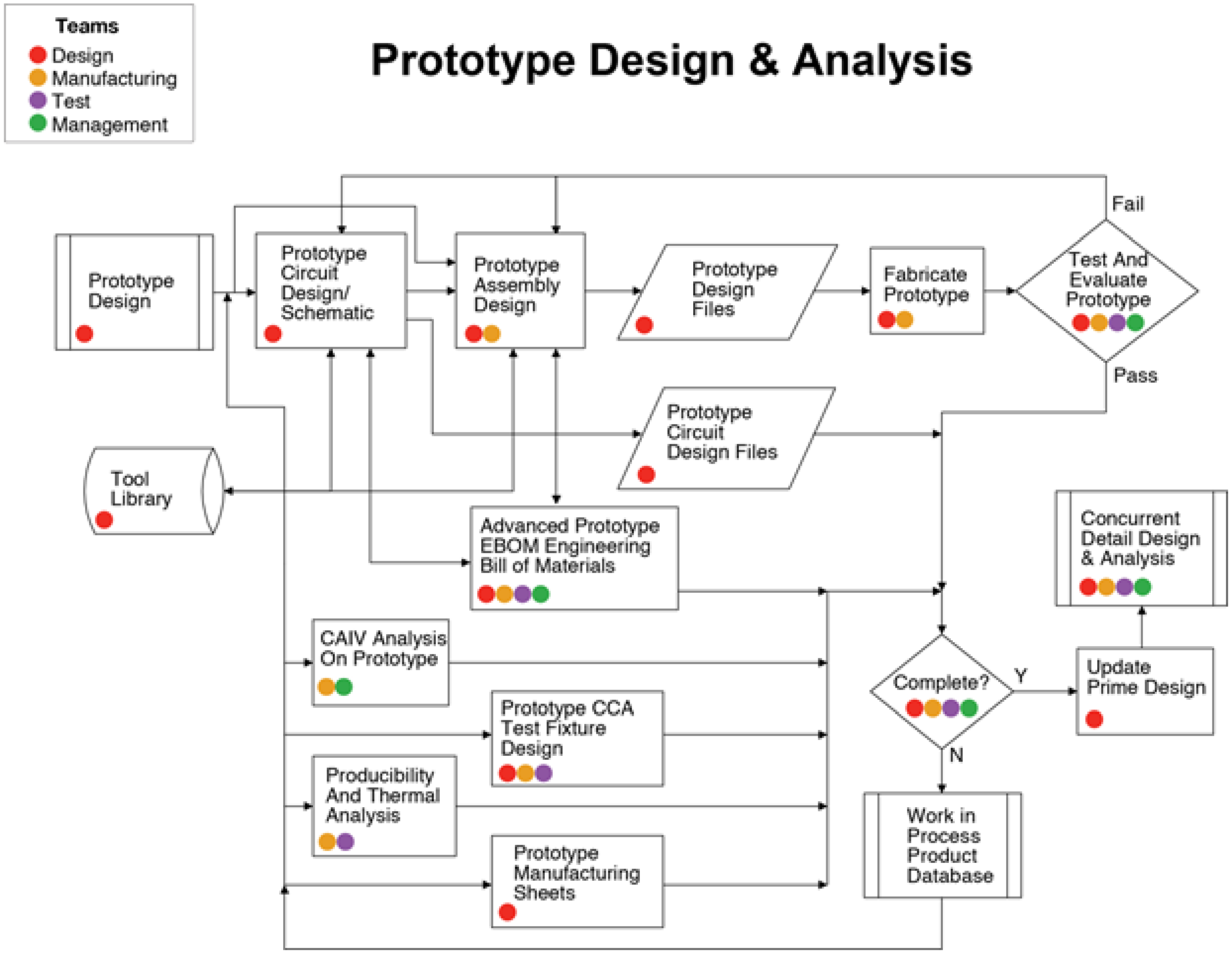
IPC-2231: The Cookbook Design for Excellence

- Very large Guideline – Best Practice Methodology
  - A “Best Practice” focus on the electronics design process commonly found in electronics hardware design life cycle through fabrication.
  - Implements detailed analysis for the Design for (X) “ilities” Manufacturability, Reliability, Testability plus additional practices.
  - Outlines a complete framework of guidelines, references, and industry standards.
  - Help the User build their own DFX Checklist
  - A unique color-coded function flow that allows user to focus on core functions related to design, manufacturing, test, or management.
  - Not intended to be read cover to cover
- Asking all IPC Committee Leaders to review the sections that are applicable to their expertise.

Example: LIFE CYCLE FLOW found in IPC -2231



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Industry Standards – IPC, JEDEC, ISO…

- Make use of existing industry standards where possible
  - Tried and true
  - Well tested and accepted
  - But – may represent only minimum acceptable requirements or concerns not relevant to your needs. Remember to modify and extend requirements as needed to customize for your product and environments!
  - Forums provide opportunities to solicit free advice and feedback on issues you face and questions you have.

IPC Design Requirement/Guideline References

- The IPC is a global trade association dedicated to the competitive excellence and financial success of all facets of the electronic interconnect industry including design, printed circuit board manufacturing and electronics assembly. http://www.ipc.org/

- Provide a forum to brings together all industry players, including designers, board manufacturers, assembly companies, suppliers, and original equipment manufacturers.

- Provides resources to:
  - Management improvement and technology enhancement
  - Creation of relevant standards
  - Protection of the environment
  - Pertinent government relations.

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Circuit Assembly Design Standards

IPC-7095A

ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES ®

Design and Assembly Process Implementation for BGAs

Developed by the Device Manufacturers Interface Committee of IPC

Supersedes:
IPC-7095 - August 2000

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1219

IPC J-STD-001D

Requirements for Soldered Electrical and Electronic Assemblies

A joint standard developed by the National Standard for Soldering Task Group (5-22a), and the Soldering Subcommittee (5-22) of the Assembly and Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:
IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1219
Phone (847) 615-7100

IPC-7711A/7721A

Rework of Electronic Assemblies

IPC-7711, Change 1 - February 2002
IPC-7711 - February 1998

Repair and Modification of Printed Boards and Electronic Assemblies

IPC-7721, Change 2 - April 2001
IPC-7721, Change 1 - March 2000
IPC-7721 - February 1998

These standards are now published in a single volume with three sections. Part 1 includes the general information and procedures that are common to both IPC-7711A and IPC-7721A. Part 2 includes all the rework procedures from IPC-7711A and Part 3 includes all the repair and modification procedures from IPC-7721A.

Developed by the Repairability Subcommittee (7-34) of the Product Assurance Committee (7-30) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135

IPC Design Requirement/Guideline References

- **IPC-2221- Generic Standard on Printed Board Design**
  - Foundation design standard for all documents in the IPC-2220 series
  - Establishes the generic requirements for the design of printed boards and other forms of component mounting or interconnecting structures
  - 3 Performance Classes
    - *Class 1 General Electronic Products -* consumer products,
    - *Class 2 Dedicated Service Electronic Products*
      - Communications equipment, sophisticated business machine, instruments and military equipment where high performance, extended life and uninterrupted service is desired but is not critical.
    - *Class 3 High Reliability Electronic Products*
      - Commercial, industrial and military products where continued performance or performance on demand is critical and where high levels of assurance are required…

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IPC Design Requirement/Guideline References

- IPC-4101 - Specification for Base Materials for Rigid and Multilayer Printed Boards
  - Covers the requirements for base materials that are referred to as laminate or prepreg. These are to be used primarily for rigid and multilayer printed boards for electrical and electronic circuits.
- IPC-7351 - Generic Requirements for Surface Mount Design and Land Pattern Standards
  - Covers land pattern design for all types of passive and active components, including resistors, capacitors, MELFs, SSOPs, TSSOPs, QFPs, BGAs, QFNs and SONs
  - Includes land pattern design guidance for lead free soldering processes, reflow cycle and profile requirements for components and new component families

IPC Design Requirement/Guideline References

- IPC-CM-770E – Component Mounting Guidelines for Printed Boards
- Provides effective guidelines in the preparation and attachment of components for printed circuit board assembly and reviews pertinent design criteria, impacts and issues
- Contains techniques for assembly (both manual and machines including SMT, BGA and flip chip) and consideration of, and impact upon, subsequent soldering, cleaning, and coating processes

IPC Design Requirement/Guideline References

- **IPC-7095 Design and Assembly Process Implementation for BGAs**
  - Provides guidelines for BGA inspection and repair, addresses reliability issues and the use of lead-free joint criteria associated with BGAs.
- **IPC J-STD-001D - Requirements for Soldered Electrical & Electronic Assemblies.**
  - J-STD-001D is world-recognized as the sole industry-consensus standard covering soldering materials and processes
    - Includes support for lead free manufacturing, in addition to easier to understand criteria for materials, methods and verification for producing quality soldered interconnections and assemblies.
  - 3 Construction Classes defined
    - Class 1 General Electronic Products
    - Class 2 Dedicated Service Electronic Products
    - Class 3 High Reliability Electronic Product
- These documents are used as a reference for the case studies and information in this workshop

Quality, Reliability & IPC Class 2 versus Class 3

- Good quality is necessary but not SUFFICIENT to guarantee high reliability
- IPC Class 3 by itself does not guarantee high reliability
  - A PCB or PCBA can be perfectly built to IPC Class 3 standards and still be totally unreliable in its final application
  - Consider two different PCB laminates both built to IPC Class 3 standards
    - Both laminates are identical in all properties EXCEPT one laminate has a CTEz of 40 (ppm/C) and the other has a CTEz of 60.
    - The vias in the laminate with the lower CTEz will be MORE reliable in a long term, aggressive thermal cycling environment than the CTEz 60 laminate.
    - A CTEz 40 laminate built to IPC class 2 could be MORE reliable than the CTEz 60 laminate built to Class 3.
    - Appropriate materials selection for the environment is key!

Commonly Used Lab Test & Reference Standards

- IPC-TM-650: Test Methods Manual
  - Series available for free download at www.ipc.org
    - http://www.ipc.org/ContentPage.aspx?PageID=4.1.0.1.1.0
      - Section 1.0:Reporting and Measurement Analysis Methods
      - Section 2.1:Visual Test Methods
      - Section 2.2:Dimensional Test Methods
      - Section 2.3:Chemical Test Methods
      - Section 2.4:Mechanical Test Methods
      - Section 2.5:Electrical Test Method
      - Section 2.6:Environmental Test Methods

ISO Standards

- ISO (International Organization for Standardization) is the world's **largest developer** and publisher of **International Standards.** www.iso.org
- ISO is a **network** of the national standards institutes of **162 countries**, one member per country, with a Central Secretariat in Geneva, Switzerland, that coordinates the system.
- ISO is a **non-governmental organization** that forms a bridge between the public and private sectors. On the one hand, many of its member institutes are part of the governmental structure of their countries, or are mandated by their government. On the other hand, other members have their roots uniquely in the private sector, having been set up by national partnerships of industry associations.
- Therefore, ISO enables a **consensus** to be reached on solutions that meet both the requirements of business and **the broader needs of society.**
- Some commonly used ISO Standards
  - ISO 9001: Quality Management Systems
  - ISO 14050: Environmental Management Systems
  - ISO 13485: Medical devices -- Quality management systems -- Requirements for regulatory purposes

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Laminate Selection

Plated Through Vias (PTVs)

PTH

Barrel Cracking

Conductive Anodic Filaments (CAF)

PCB Materials & Laminate Selection

- Laminate selection is frequently under specified! Some common issues:
  - PCB supplier frequently allowed to select laminate material
  - No restrictions on laminate changes
  - Generic IPC slash sheet requirements used
  - Laminates called out by Tg only and with no measurement method specified
    - There is more than one!
  - No cleanliness requirements specified
  - Failure to specify stackup
- Not all laminates are created equal
  - Failure to put some controls in places opens the door to failure

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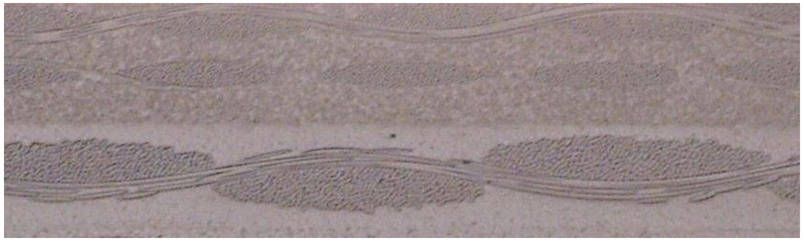
PCB Materials and Reliability

- Historically, two material properties of concern
  - Out-of-plane coefficient of thermal expansion (CTE_z)
  - Out-of-plane elastic modulus ('stiffness')(E_z)

- Key Assumption: No exposure to temperatures above the glass transition temperature (Tg)

- The two material properties (CTE and E) are driven by choices in resin, glass style, and filler



PCB Robustness: Laminate Material Selection

Board thickness	IR-240~250°C	Board thickness	IR-260°C
≤60mil	Tg140 Dicy All HF materials OK	≤ 60mil	Tg150 Dicy HF- middle and high Tg materials OK
60~73mil	Tg150 Dicy NP150, TU622-5 All HF materials OK	60~73mil	Tg170 Dicy HF –middle and high Tg materials OK
73~93mil	Tg170 Dicy, NP150G-HF HF –middle and high Tg materials OK	73~93mil	Tg150 Phenolic + Filler IS400, IT150M, TU722-5, GA150 HF –middle and high Tg materials OK
93~120mil	Tg150 Phenolic + Filler IS400, IT150M, TU722-5 Tg 150 HF –middle and high Tg materials OK	93~130mil	Phenolic Tg170 IS410, IT180, PLC-FR-370 Turbo, TU722-7 HF –middle and high Tg materials OK
121~160mil	Phenolic Tg170 IS410, IT180, PLC-FR-370 Turbo TU722-7 HF –high Tg materials OK	≧131mil	Phenolic Tg170 + Filler IS415, 370 HR, 370 MOD, N4000-11 HF –high Tg materials OK
≧161mil	PhenolicTg170 + Filler IS415, 370 HR, 370 MOD, N4000-11 HF material - TBD	≧161mil	TBD – Consult Engineering for specific design review

1. Copper thickness = 2OZ use material listed on column 260 °C
2. Copper thickness >= 3OZ use Phenolic base material or High Tg Halogen free materials only
3. **Twice lamination product use Phenolic material or High Tg Halogen free materials only (includes HDI)**
4. Follow customer requirement if customer has his own material requirement
5. DE people have to confirm the IR reflow Temperature profile

J. Beers, Gold Circuits

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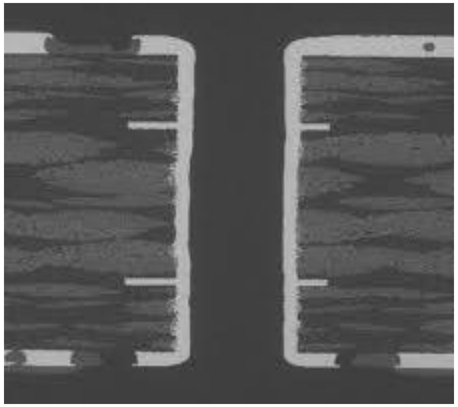
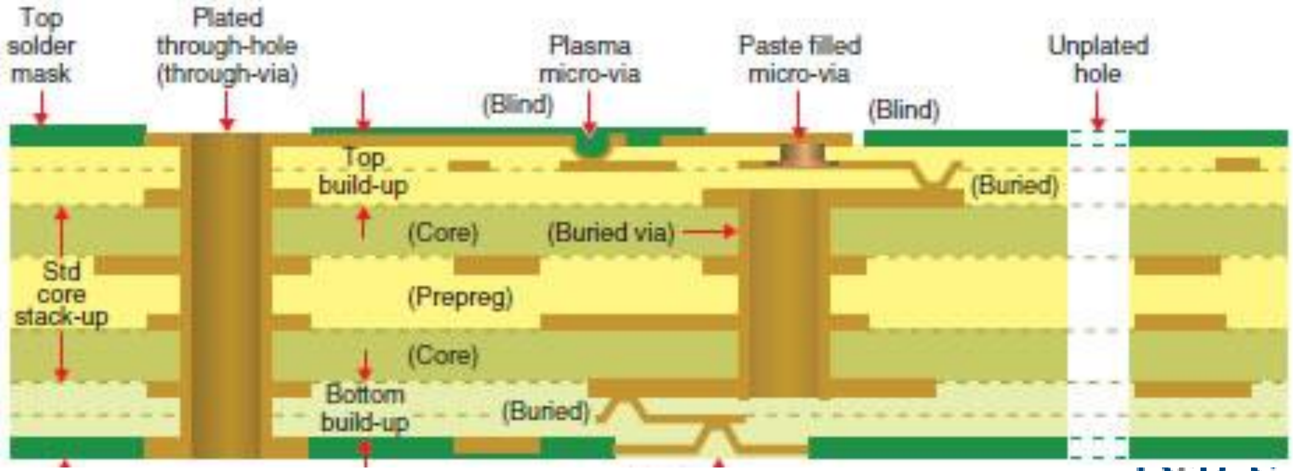
Reliable Plated Through-Via Design and Fabrication

What is a Plated Through Via?

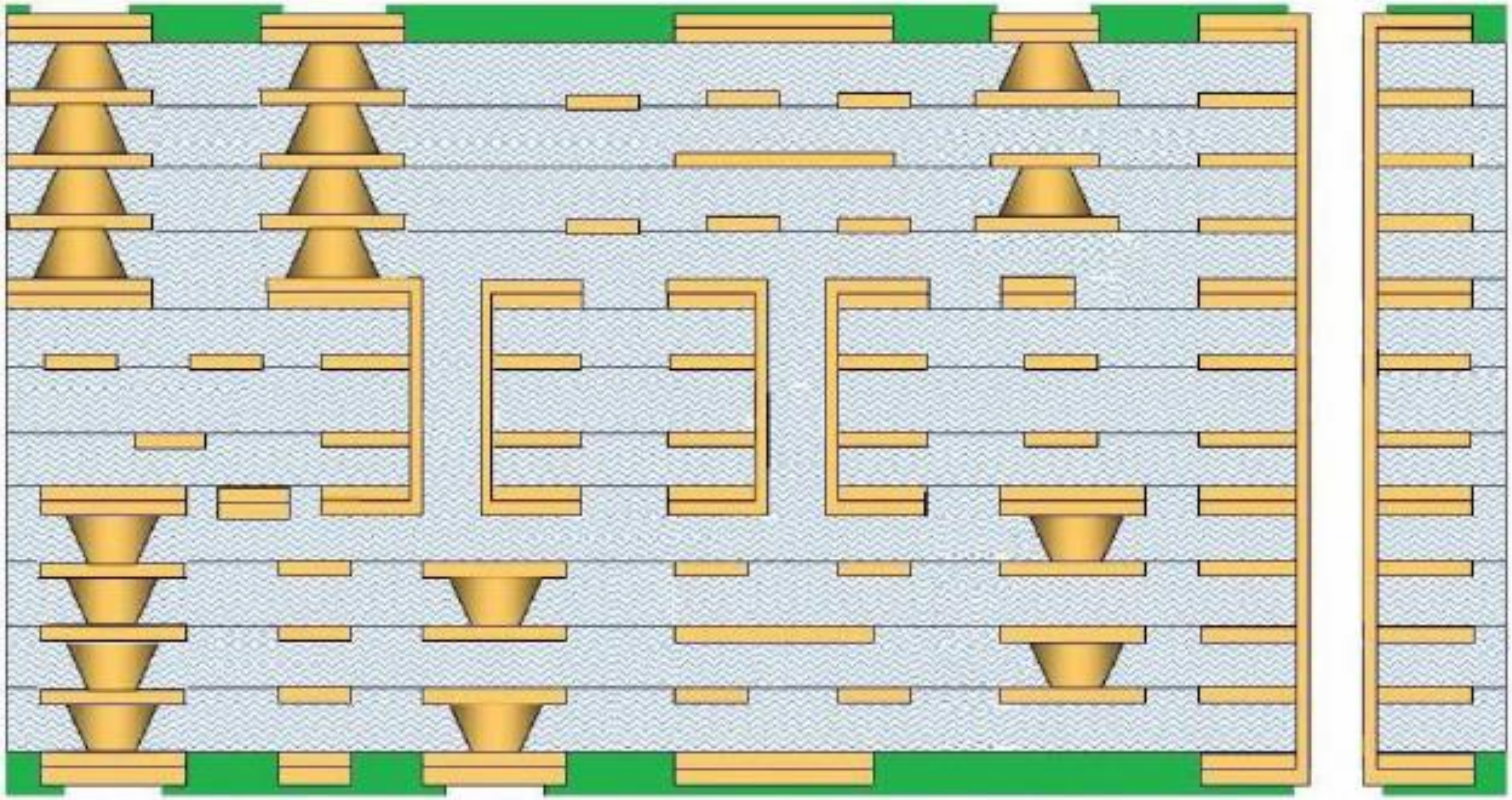
- A plated through via (PTV) is an interconnect within a printed circuit board (PCB) that electrically and/or thermally connects two or more layers



- PTV is part of a larger family of interconnects within PCBs



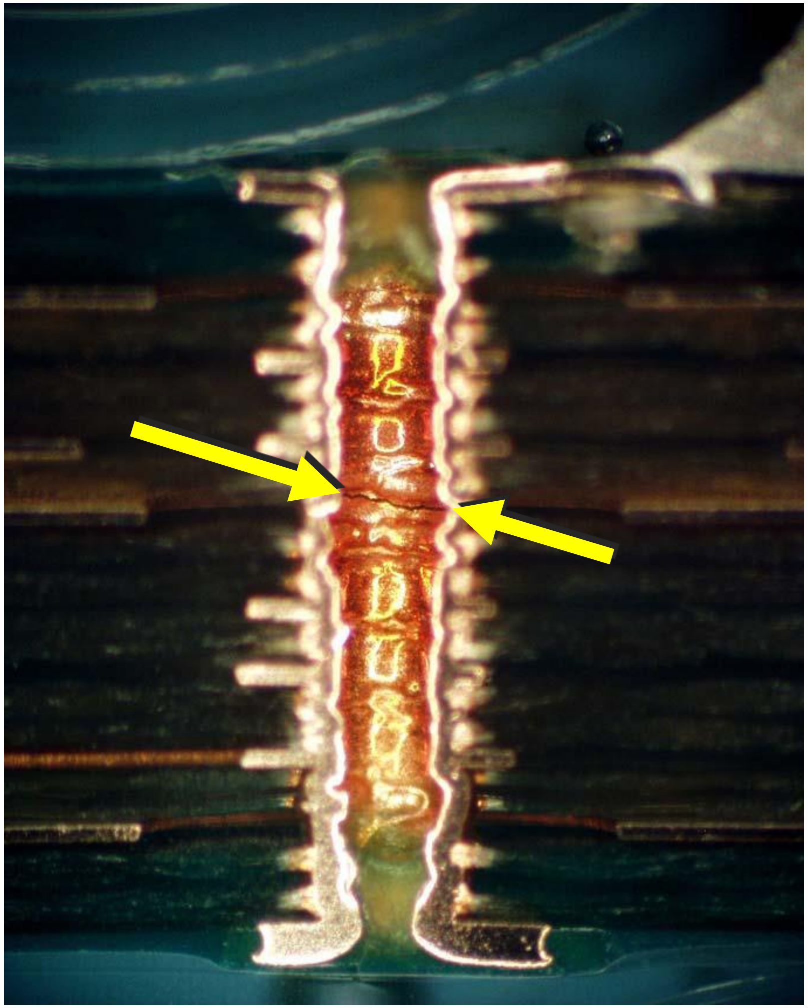
PCB Vias



DfR Solutions

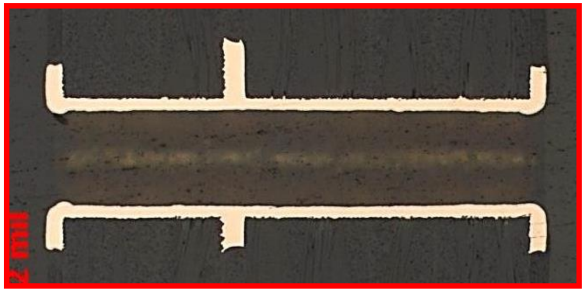
How do PTV's Fail?

- The dominant failure mode in PTV tends to be barrel fatigue
- Barrel fatigue is the circumferential cracking of the copper plating that forms the PTV wall
- Driven by differential expansion between the copper plating (~17 ppm/C) and the out-of-plane CTE of the printed board (~70 ppm/C)



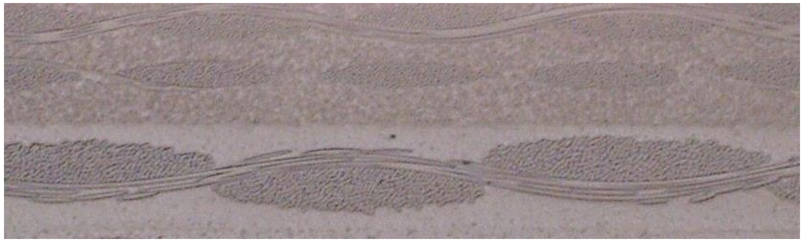
How to Design a Reliable PTV?

PTH Architecture
(height / diameter)



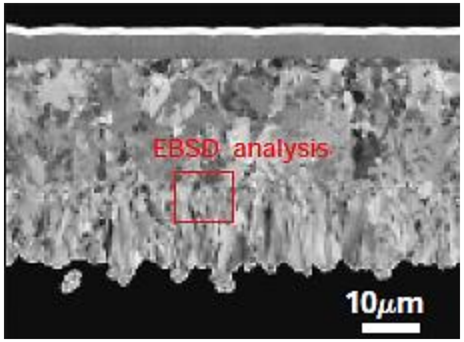
+

PCB Material
(modulus / CTE)



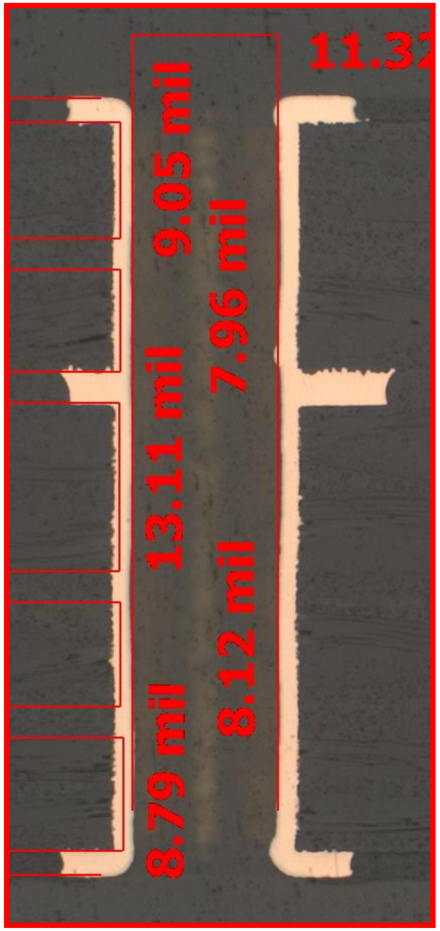
+

Plating
(thickness / material)



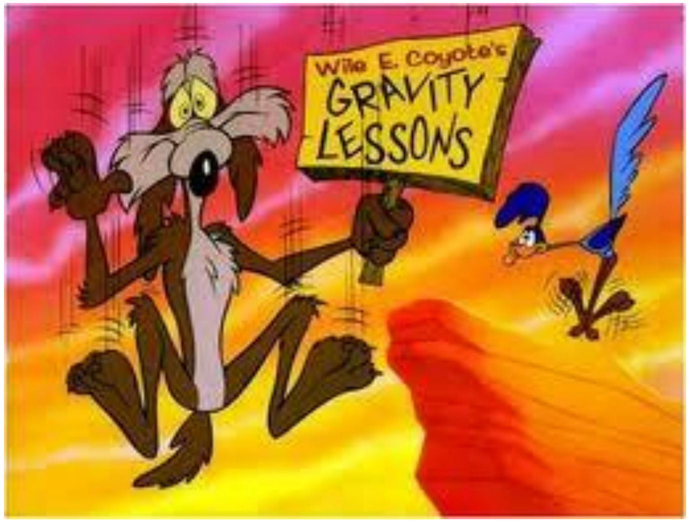
PTV Architecture

- PTV Height
  - Driven by the PCB thickness
  - 30 mil (0.75 mm) to 250 mil (6.25 mm)
- PTV Diameter
  - Driven by component pitch/spacing
  - 6 mil (150 micron) to 20 mil (500 micron)
- Key Issues
  - Be aware that PCB manufacturing has cliffs
  - Quantify effect of design parameters using IPC TR-579



DfR Solutions

The PTV Cliff



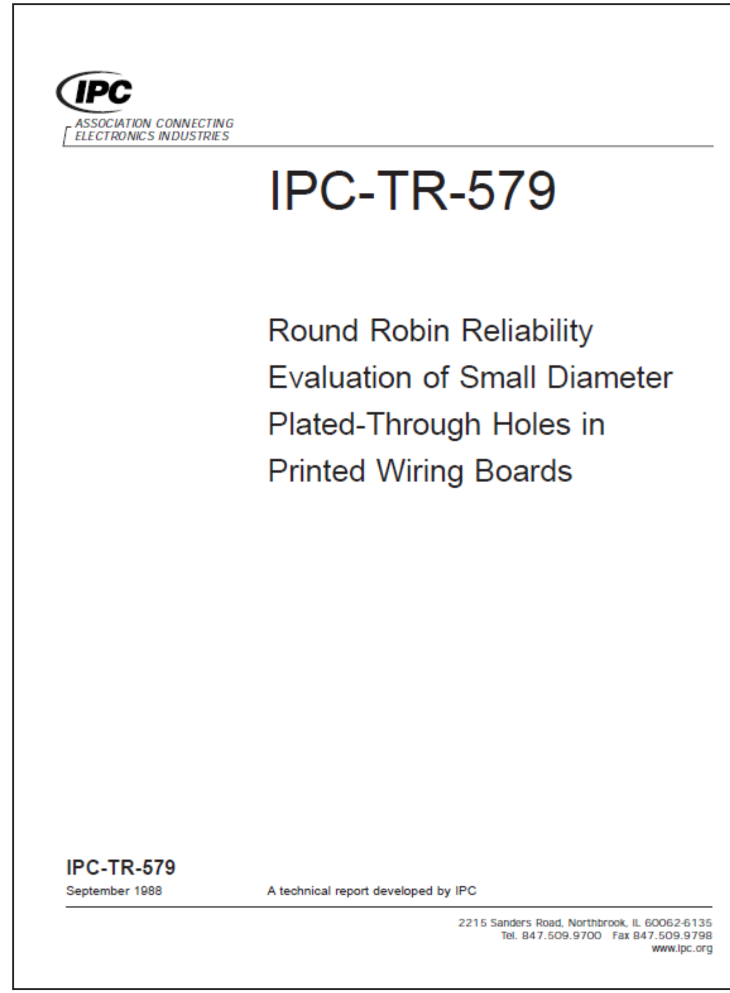
- Data from 26 PCB manufacturers
- Wide range of PCB designs
  - 6 to 24 layer
  - 62 to 125 mil thickness
- Results after six lead-free reflows
  - Initial defects segregated

Process Attribute	Hole/land (mils)	Count	Min	Q1	Median	Q3	Max
Yield Loss from Assembly Simulation (%) Threshold: Open	8 / 18	6	0.00	0.00	0.31	3.24	17.16
	10 / 20	15	0.00	0.00	0.00	1.13	4.60
	12 / 22	26	0.00	0.00	0.00	0.00	5.23
	13.5 / 23.5	26	0.00	0.00	0.00	0.00	4.09
	14.5 / 24.5	19	0.00	0.00	0.00	0.00	0.00
	16 / 26	11	0.00	0.00	0.00	0.00	0.00

Courtesy of CAT

IPC TR-579

- Round Robin Reliability Evaluation of Small Diameter (<20 mil) Plated Through Holes in PWBs
- Activity initiated by IPC and published in 1988
- Objectives
  - Confirm sufficient reliability
  - Benchmark different test procedures
  - Evaluate influence of PTH design and plating (develop a model)


IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

IPC-TR-579

Round Robin Reliability Evaluation of Small Diameter Plated-Through Holes in Printed Wiring Boards

IPC-TR-579
September 1988

A technical report developed by IPC

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org

Assessment of IPC-TR-579

- Advantages
  - Analytical (calculation straightforward)
  - Validated through testing
  - Provides guidance on relative influence of design/material parameters

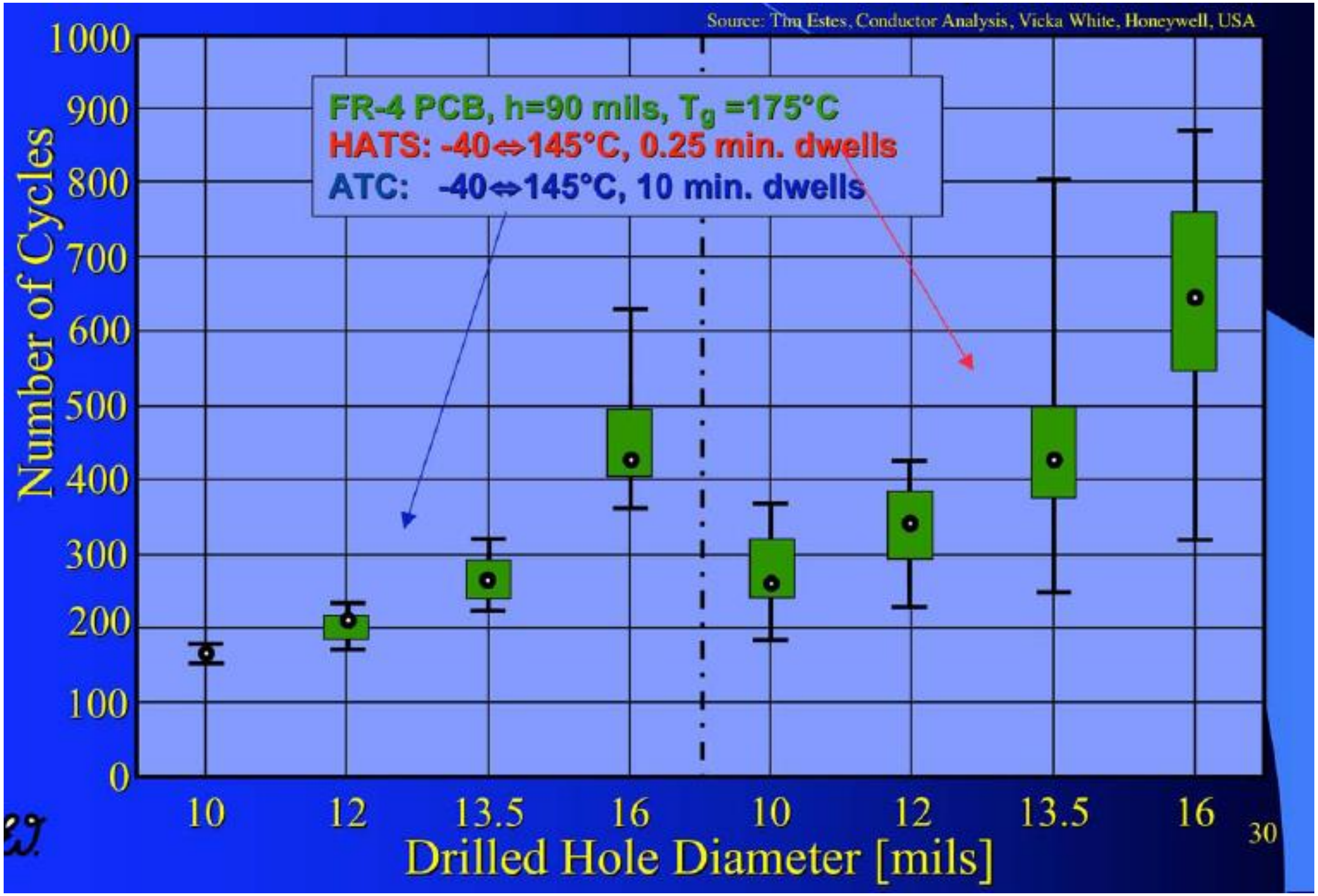
- Disadvantages
  - No ownership
  - Validation data is ~18 years old
  - Unable to assess complex geometries (PTH spacing, PTH pads)
    - Complex geometries tend to extend lifetime
  - Difficult to assess effect of multiple temperature cycles
    - Can be performed using Miner's Rule
  - Simplified assumptions (linear stress-strain above yield point)
  - How does one determine the quality index in the design phase?
  - Does not account for the effect of fill
  - Does not consider other failure modes (knee cracking, wall-pad separation, etc.)

The Effect of Design Parameters (Height / Diameter)

- Reduce the PTV Height (PCB Thickness)
  - Reduce laminate/prepreg thickness (2.7 to 4 mil is current limitation)
  - Results in minimal cost changes and minimal effect on design
  - Has the least effect on PTH reliability
- Increase PTV Diameter
  - Typically not an option due to spacing issues
  - An important, but significant effect (dependent on a number of other variables)
  - Example: Moving from 10 mil to 12 mil diameter on a 120 mil board, 50C temp cycle, will result in approximately 20% improvement

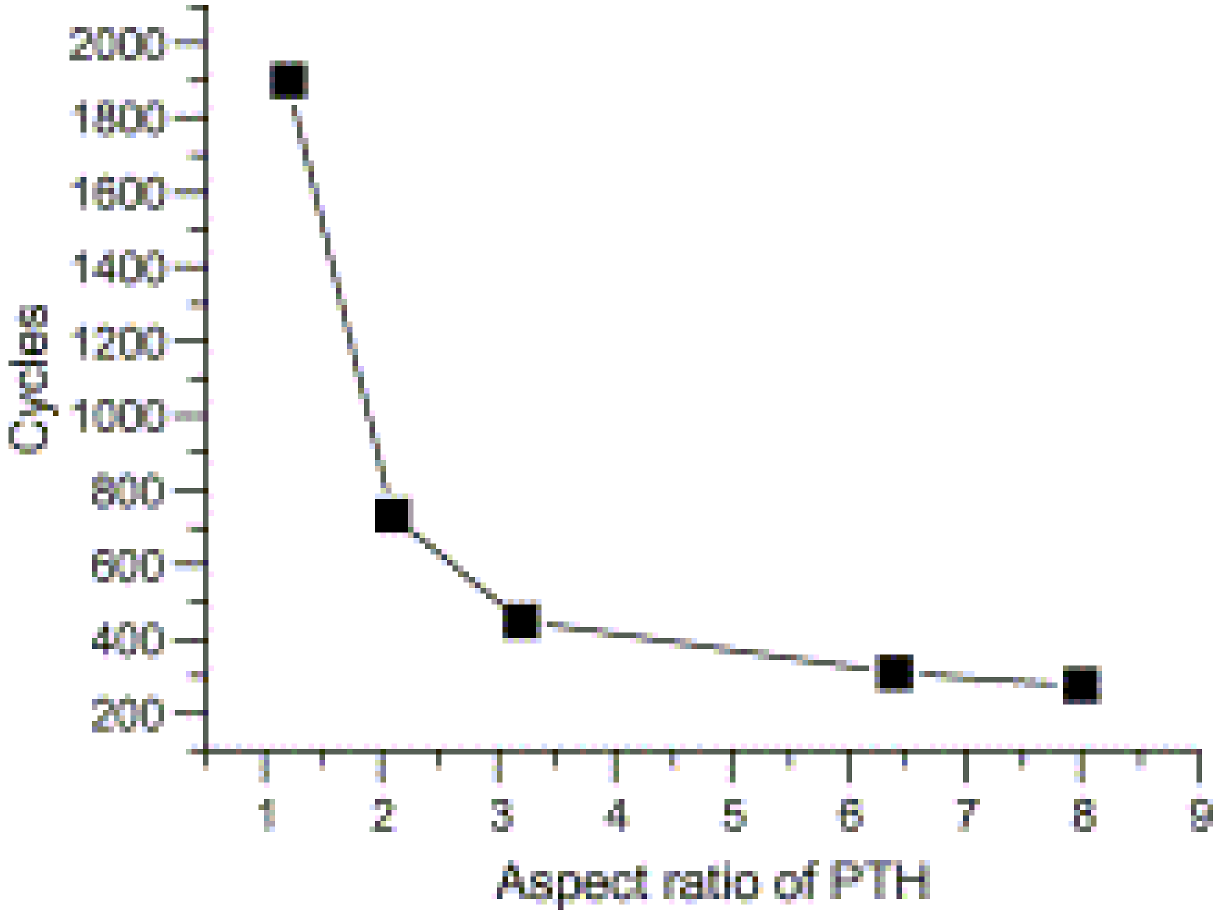
DfR Solutions

Effect of Design Parameters (cont.)



W. Engelmaier, Reliability Issues for Printed Circuit Boards in Lead-Free Soldering

Effect of Design Parameters (cont.)



DfR Solutions

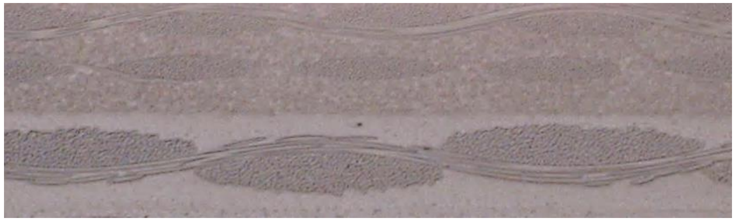
F. Su, et. al., Microelectronics Reliability, June 2012

PCB Materials and PTV Reliability

- Historically, two material properties of concern
  - Out-of-plane coefficient of thermal expansion (CTE_z)
  - Out-of-plane elastic modulus ('stiffness')(E_z)

- Key Assumption: No exposure to temperatures above the glass transition temperature (Tg)

- The two material properties (CTE and E) are driven by choices in resin, glass style, and filler



DfR Solutions

Laminate Datasheets

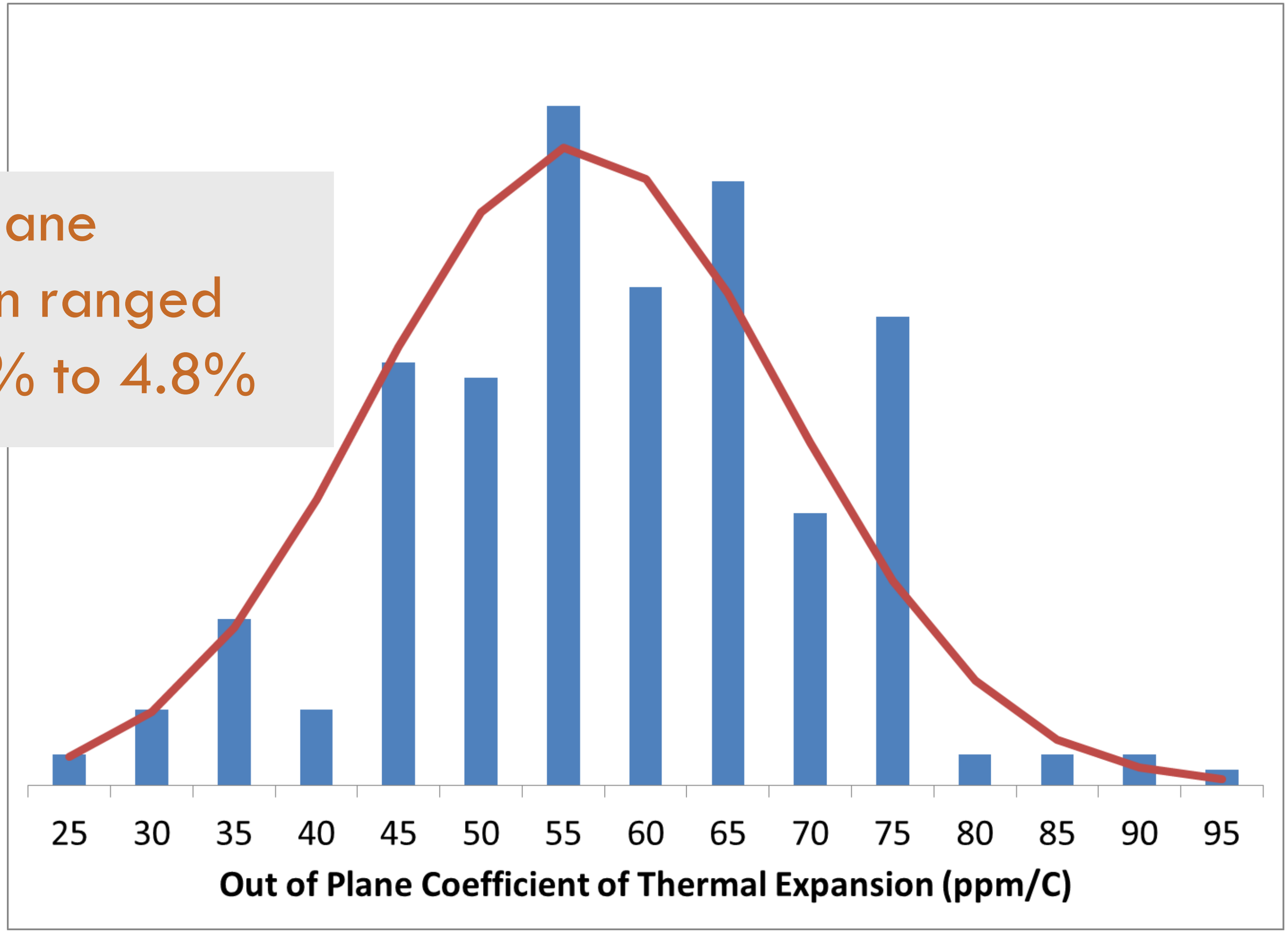
- Out-of-plane CTE (CTEz) is almost always provided on the laminate datasheet
  - Sometimes in ppm/C above and below the Tg
  - Sometimes in % between 50-260C
- Out-of-plane modulus (Ez) is almost never provided on the laminate datasheet
  - Requires calculation based on in-plane laminate properties, glass fiber properties, glass fiber volume fraction, and Rule-of-Mixtures / Halpin-Tsai models

$$1/E_{laminate} = V_{epoxy}/E_{epoxy} + V_{fiber}/E_{fiber}$$

DfR Solutions

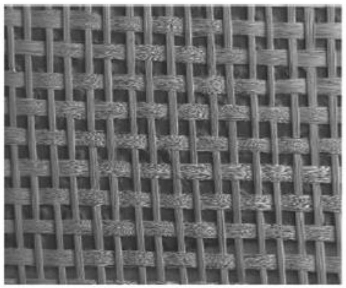
Survey of 300 Different FR-4 Datasheets

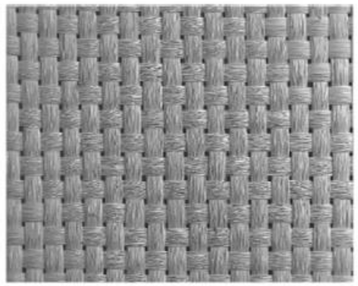
- Out-of-plane expansion ranged from 1.4% to 4.8%

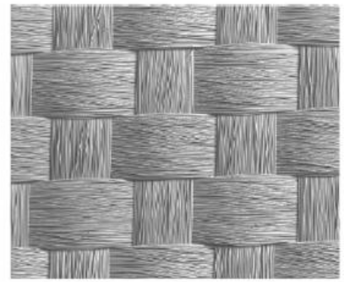


Glass Style

- PCB laminates (and prepregs) are fabricated with a variety of glass styles


1080


2116


7628

- Problem: All datasheet properties are for laminate with 7628 glass style
  - Most laminate (and all prepreg) in complex PCBs have a low volume fraction of glass (i.e., 1080 or 106)

Glass Style	Resin Volume Content	Fiber Volume Content
1027	0.86	0.14
1037	0.86	0.14
106	0.84	0.16
1067	0.84	0.16
1035	0.83	0.17
1078	0.82	0.18
1080	0.79	0.21
1086	0.78	0.22
2313	0.74	0.26
2113	0.72	0.28
2116	0.71	0.29
3313	0.71	0.29
3070	0.68	0.32
1647	0.66	0.34
1651	0.66	0.34
2165	0.66	0.34
2157	0.66	0.34
7628	0.64	0.36

Glass Style and CTE

Glass Style	Modulus of Elasticity Ez (MPa)	CTEz (ppm/C)
1027	4380.4	73.9
1037	4380.4	73.9
106	4478.2	72.3
1067	4478.2	72.3
1035	4528.7	71.5
1078	4580.3	70.7
1080	4742.7	68.4
1086	4799.3	67.6
2313	5040.4	64.4
2113	5170.2	62.8
2116	5237.6	62.0
3313	5237.6	62.0
3070	5450.9	59.7
1647	5603.1	58.1
1651	5603.1	58.1
2165	5603.1	58.1
2157	5603.1	58.1
7628	5764.0	56.5

Laminate Properties (cont.)

- More recently, additional laminate properties of concern due to Pb-free assembly
  - Glass transition temperature (Tg)
  - Time to delamination (T260, T280, T288, T300)
  - Temperature of decomposition (Td)

- Each parameter 'supposedly' captures a different material behavior
  - Higher number slash sheets (> 100) within IPC-4101 define these parameters to specific material categories

Thermal Parameters of Laminate

- Glass transition temperature (Tg) (IPC-TM-650, 2.4.24/2.4.25c)
  - Characterizes complex material transformation (increase in CTE, decrease in modulus)
- Time to delamination (T-260/280/288/300) (IPC-TM-650, 2.4.24.1)
  - Characterizes interfacial adhesion
- Temperature of decomposition (Td) (IPC-TM-650, 2.3.40)
  - Characterizes breakdown of epoxy material

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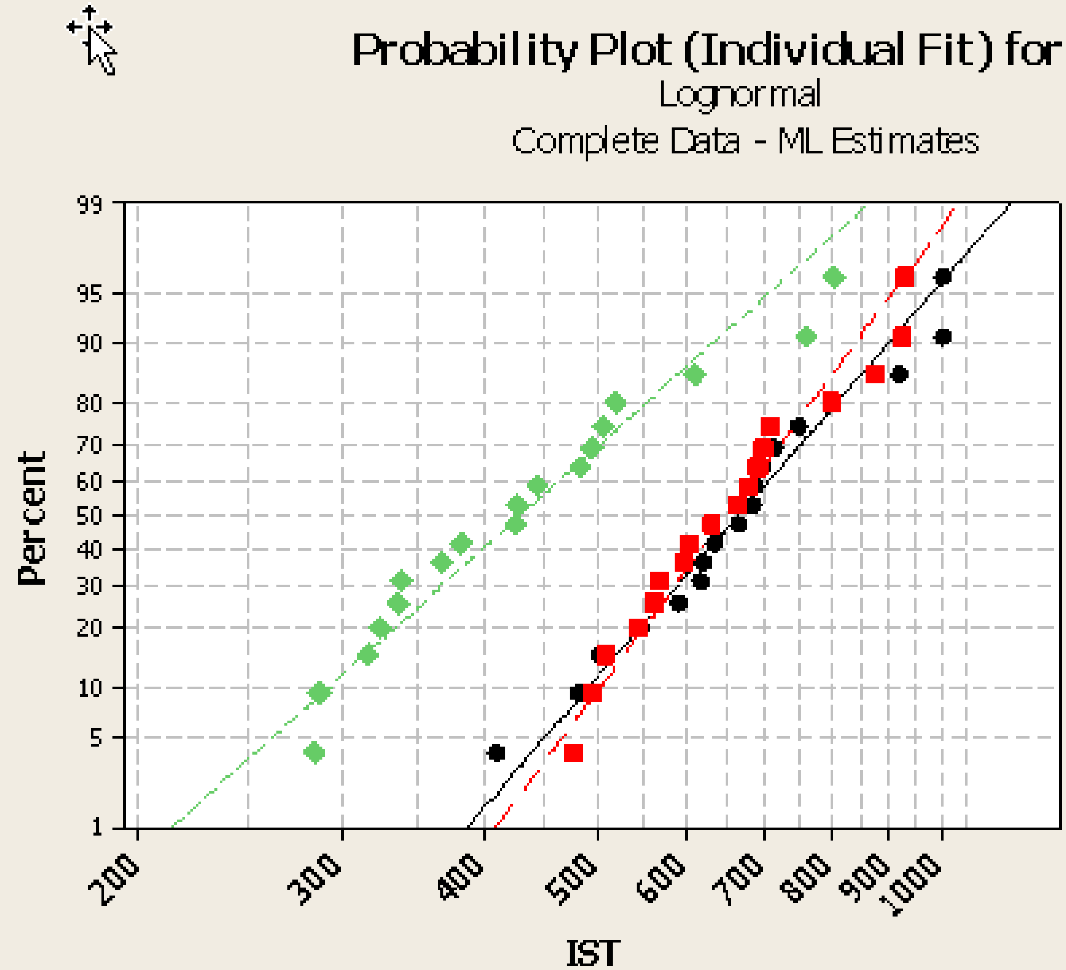
Thermal Parameters and IPC Slash Sheets

IPC-4101	99	101	102	103	121	122	124	125	126	127	128	129	130	131
ANSI	FR4	FR4	PPE	PPO	FR4	HF-FR4	FR4	HF-FR4	FR4	HF-FR4	HF-FR4	FR4	HF-FR4	HF-FR4
Fillers > 5%	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	Yes	Yes	Yes	N/A	Yes	N/A
Tg	>150° C	>110° C	>185° C	>150° C	>110° C	>110° C	>150° C	>150° C	>170° C	>110° C	>150° C	>170° C	>170° C	>170° C
Td	>325° C	>310° C	>340° C	>325° C	>310° C	>310° C	>325° C	>325° C	>340° C	>310° C	>325° C	>340° C	>340° C	>340° C
CTE 50-260°C	<3,5 %	<4%	<2,8 %	<3,5 %	<4%	<4%	<3,5 %	<3,5 %	<3,0 %	<4%	<3,5 %	<3,5 %	<3,0 %	<3,5 %
T260	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min
T288	>5 min	>5 min	>15 min	>5 min	>5 min	>5 min	>5 min	>5 min	>15 min	>5 min	>5 min	>15 min	>15 min	>15 min
T300	---	---	>2 min	---	---	---	---	---	>2 min	---	---	>2 min	>2 min	>2 min

HDI Printed Circuit Boards, NCAB Group

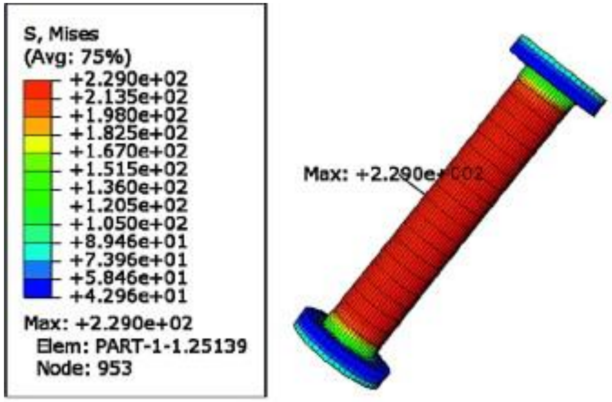
PTV Degradation due to Assembly



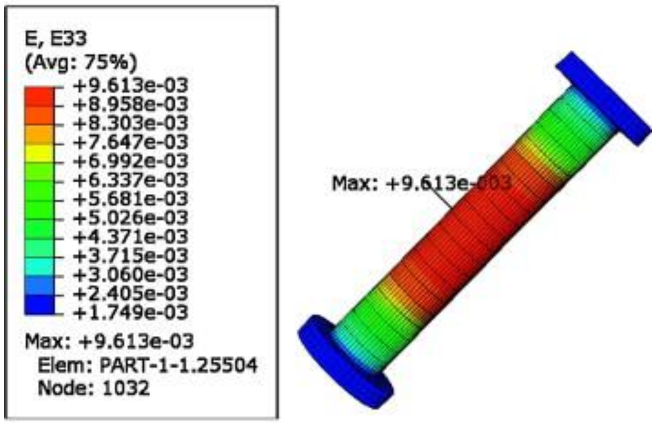
Loc	Scale	AD*	F	C
6.50154	0.233073	0.939	18	0
6.47937	0.198977	0.999	18	0
6.06531	0.299126	1.038	18	0

PCB Materials: Stackup

- Maximum stress in the PTV during thermal cycling tends to be in the middle of the barrel
- There is some concern that areas of high resin content in the middle of the barrel can be detrimental
- Non-functional pads (NFP)
  - Some debate as to their influence on barrel fatigue on higher aspect ratio PTV



(a) The Mises stress field of PTH at 150°C



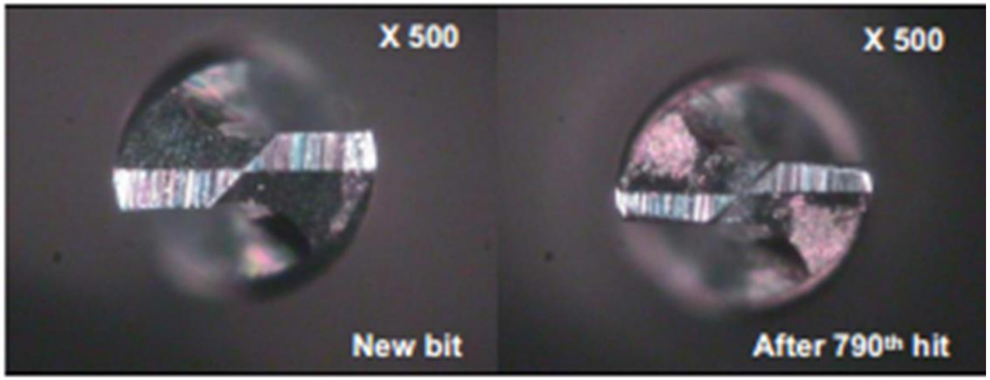
(b) The residual strain field of PTH after 3 cycles

F. Su, et. al., Microelectronics Reliability, June 2012

DfR Solutions

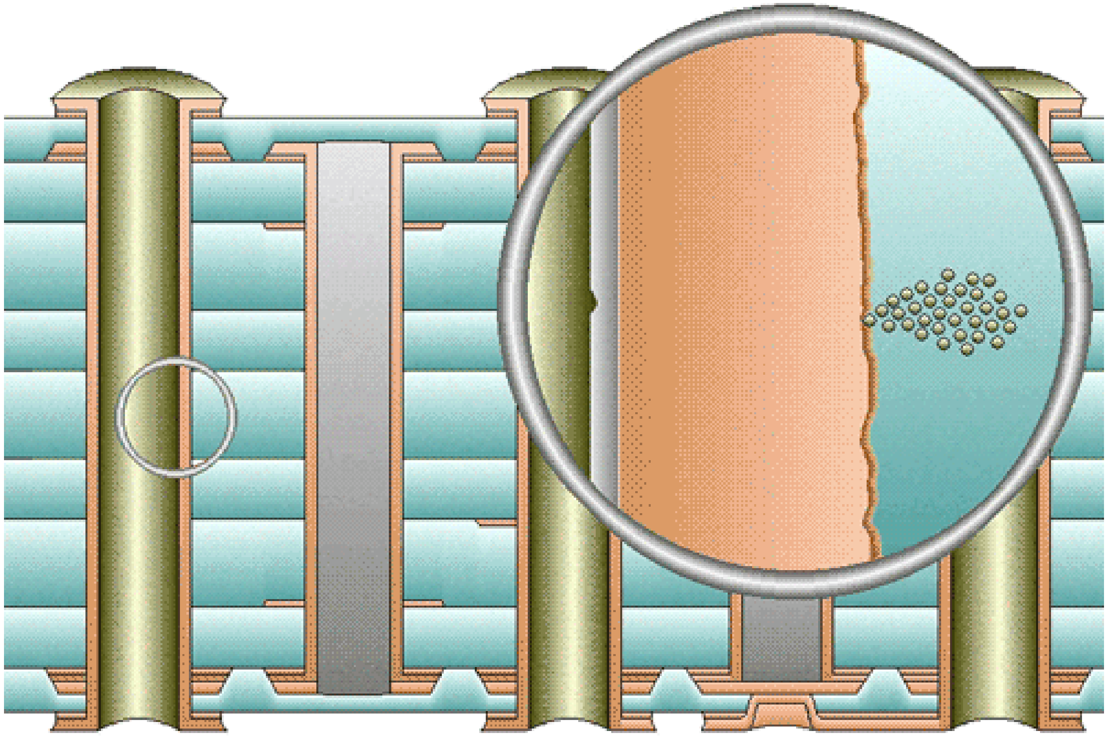
Why Remove NFPs?

- Reduce drill wear
- Faster automated optical inspection (AOI)
  - Less features to review
- Reduce shorts / Improve clearance / Reduce misregistration
  - Tight registration
  - Spacing
  - Improves yields
    - Reduces cost



Drilling Burr Minimization and Energy Saving for PCB Production, LMAS 2011

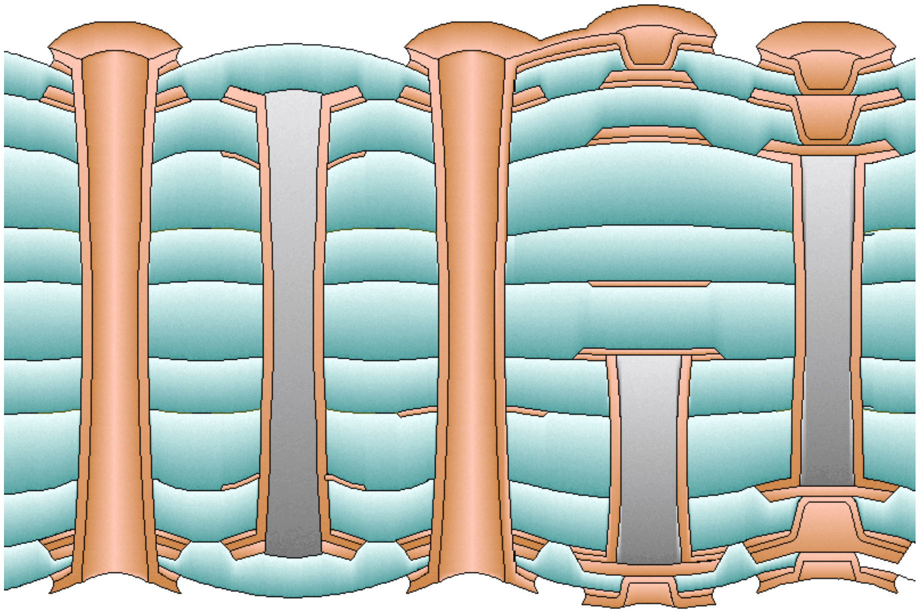
CTE Z Axis



DfR Solutions

Why Keep NFPs?

- Concern for accidental removal of a functional pad
- Belief that they anchor the hole & improve reliability
- More copper that can be retained on any layer, the better the dimensional stability

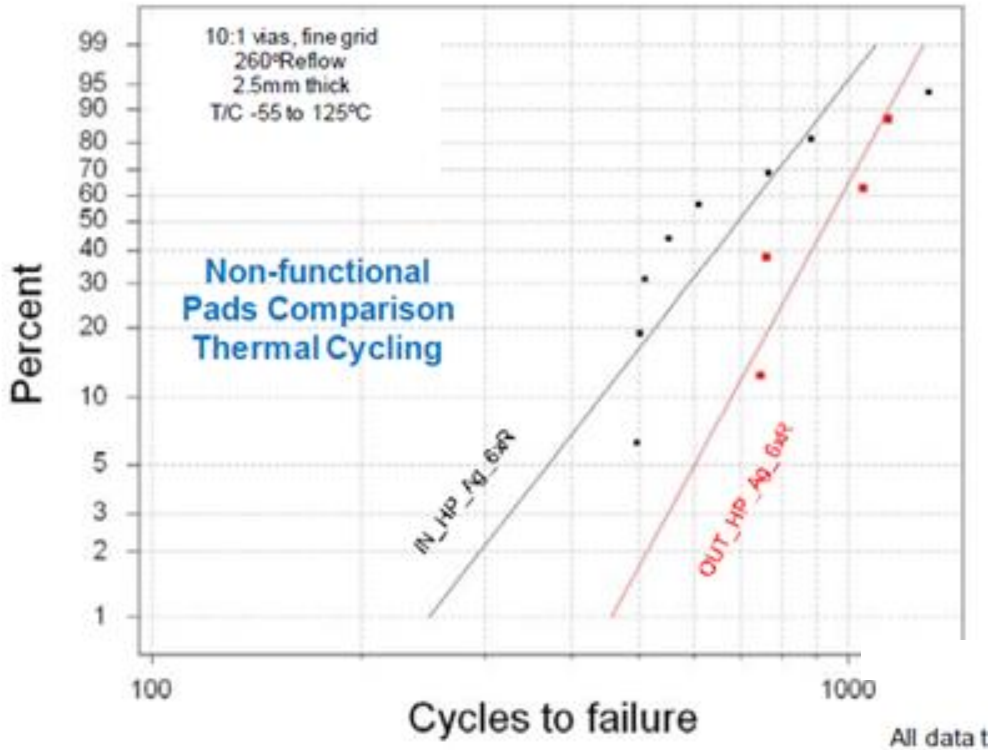


Cross Section of Typical Interconnections at 260C,

Design and Construction Affects on PWB Reliability, PWB Interconnect Solutions

NFPs & PTH Reliability for High Aspect Via Holes

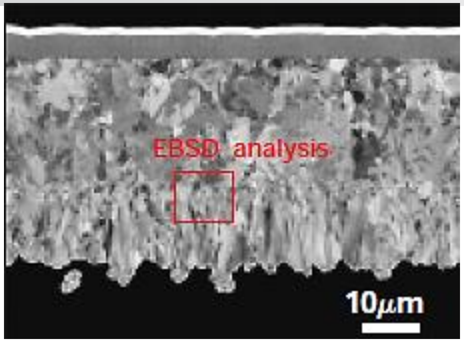
- NPL reported higher percentage and earlier fails of vias with NFPs
  - Black Line is NFPs IN
  - Red Line is NFPs OUT



[2] Wickham Martin, “Through Hole Reliability for High Aspect Via Holes,” NPL Webinar June 11, 2013

DfR Solutions

Plating (Thickness and Material Properties)

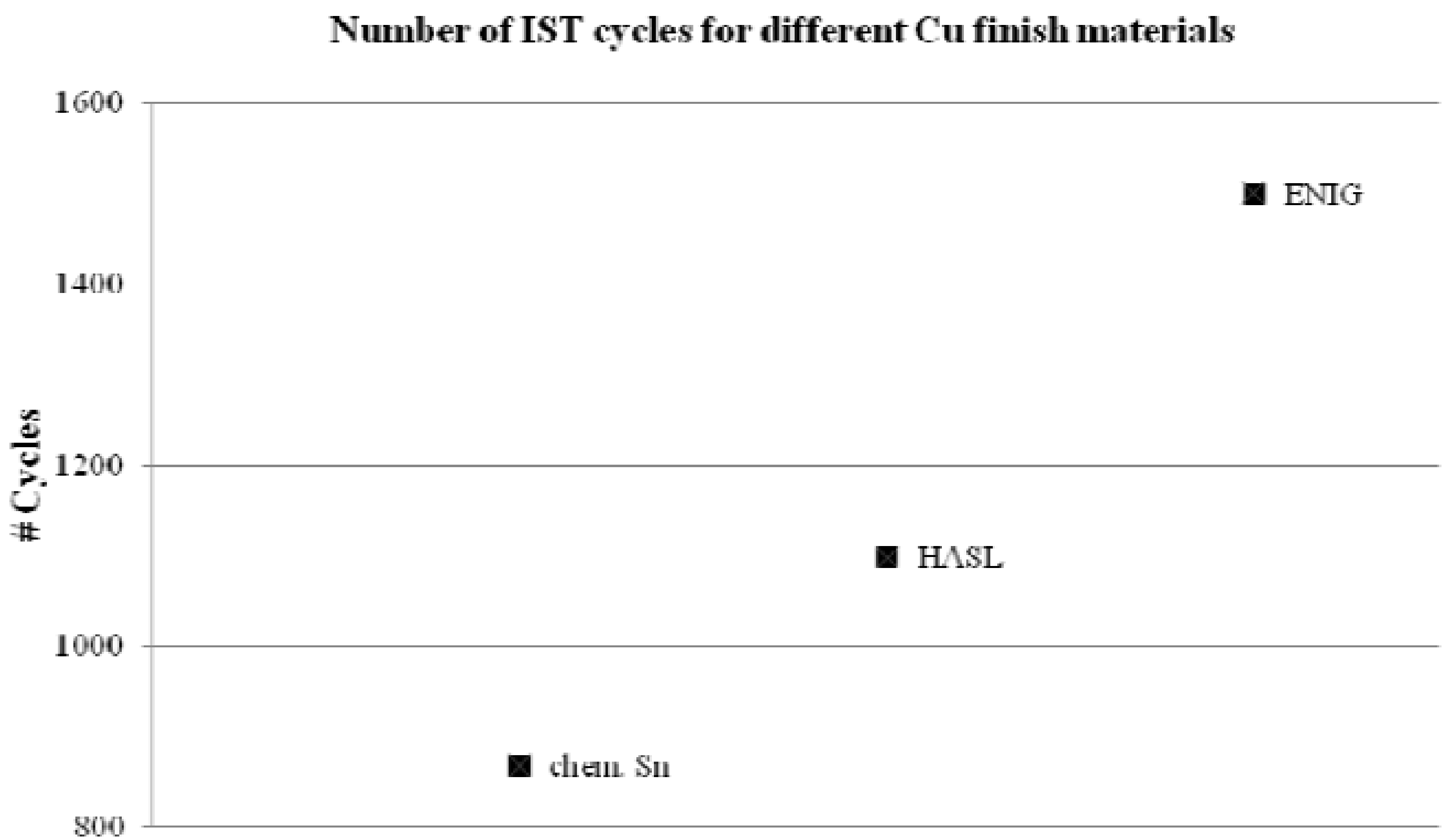


- Considered to be the number one driver for PTV barrel fatigue
- Classic engineering conflict
  - Better properties (greater thickness, higher plating strength, greater elongation) typically require longer time in the plating bath
  - Longer time in the plating bath reduces throughput, makes PCBs more expensive to fabricate
- PCB fabricators, low margin business, try to balance these conflicting requirements
  - Key parameters are thickness, strength, and elongation (ductility)

The Reality of PTV Performance (cont.)

- PCB Manufacturers tend to be very aware of test requirements specified by larger/higher reliability customers
  - Plating conditions are adjusted to meet the test requirements of those industries / customers
  - Moral of the story: Use a supplier with many high reliability customers!

Other Platings (cont.)



- S. Neumann, Theoretical and Practical Aspects of Thermo Mechanical Reliability in Printed Circuit Boards with Copper Plated Through Holes

How to Manufacture a Reliable PTV?

Drilling

\+

Plating

Hole preparation (desmear / electroless / direct metal) is important, but not as critical as drilling and electrolytic plating

DfR Solutions

Drilling

- Drill bit manufacturers tend to provide PCB manufacturers recommendations on key process parameters
  - Speeds and feeds
  - Stackup guidelines (number of PCBs of a given thickness that can be stacked during drilling)
  - Entry and exit material
  - Number of drilling operations before repointing
  - Number of repoints / sharpening

- There is no 'right' answer for process parameters
  - PCB manufacturer may buy a more expensive drill bit, but repoint more often

DfR Solutions

Plating (Electrolytic)

- Like drilling, plating chemistry manufacturers provide PCB manufacturers with guidance on process parameters & equipment
  - Many provide 'turn-key' installation
  - Can result in a lack of knowledge if PCB manufacturers do not perform their own DoE
- Large variation in plating chemistries, process and equipment

DfR Solutions

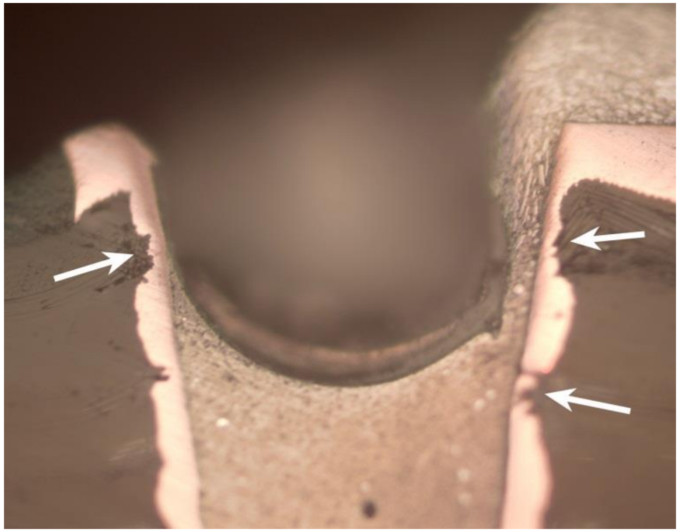
Insufficient Plating Thickness

- ANSI/IPC-A-600 requires an average plating thickness of 20 um
- Caused by
  - Insufficient current/time in the copper plating bath
  - Poor throwing power
- When observed throughout the PTH, instead of just at the center, root-cause is more likely insufficient current/time in the plating bath

DfR Solutions

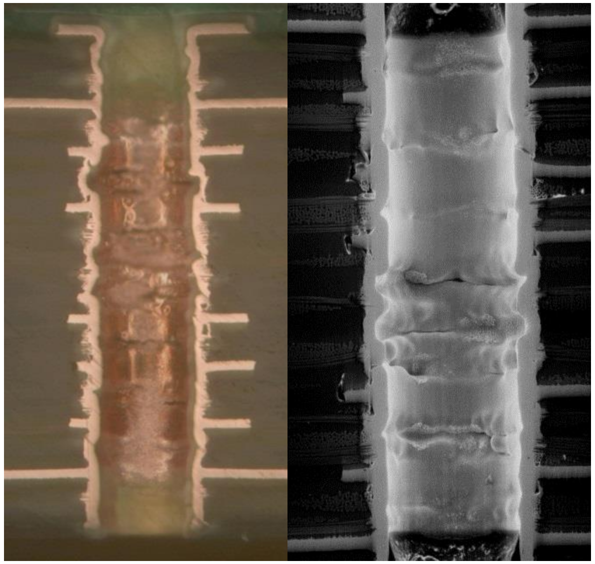
Glass Fiber Protrusion

- Affects PTH plating thickness & can contribute to PTH cracking
- May be due to
  - Process control
  - Variabilities during hole drilling
  - Hole preparation or application of flash copper.
- Allowed by IPC guidelines only if the min. plating thickness is met



Plating Folds

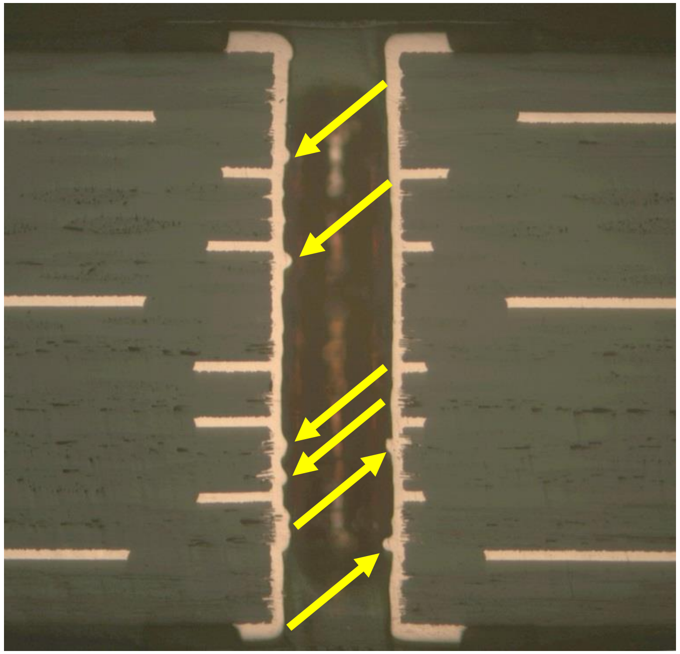
- Create stress concentrations
- Rough drilling or improper hole preparation can cause
  - Rough drilling can be caused by
    - Poor laminate material
    - Worn drill bits
    - Out-of-control drilling process
  - Improper hole preparation can be due to
    - Excessive removal of epoxy resin caused by incomplete cure of resin system
    - Un-optimized desmear/etchback process



DfR Solutions

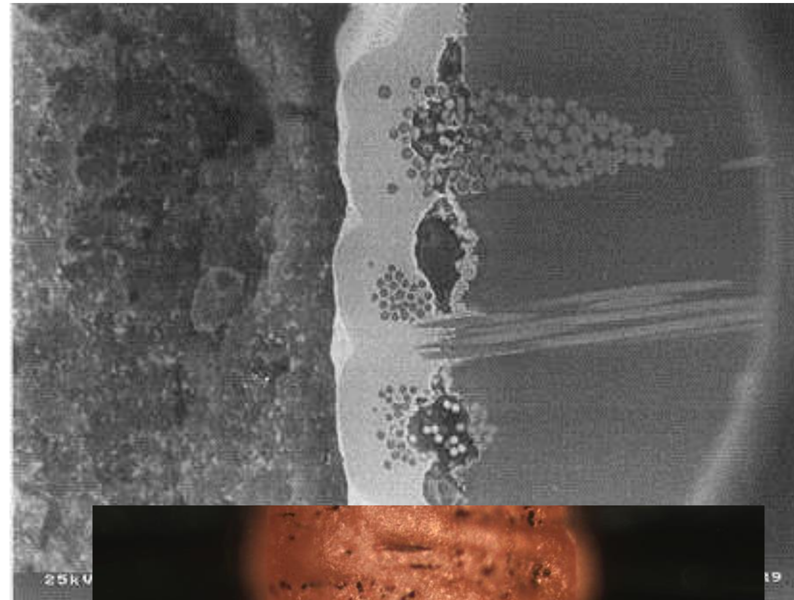
Plating Nodules

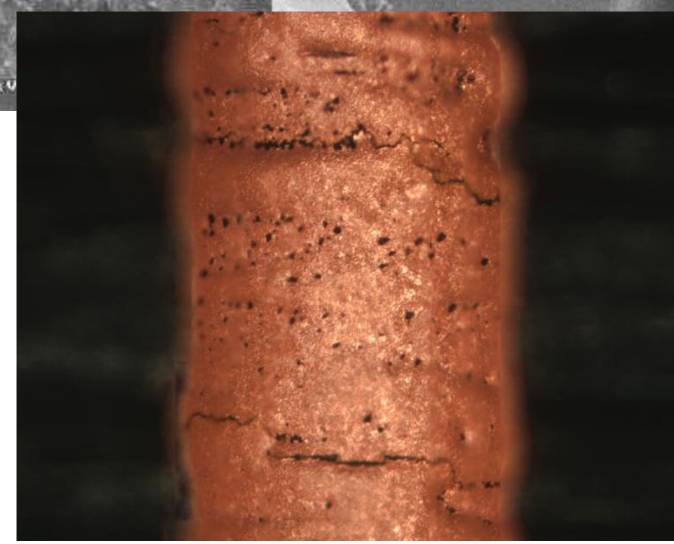
- Root causes include
  poor drilling, particles in solution, solution temperature out of range, or excess brightener level
  - Relatively straight hole walls and the lack of particles in the nodules seemed to suggest the later two as root cause in the image
- Creates highly stressed areas in the plating wall and can possibly reduce lifetime under temperature cycling.
- ANSI/IPC-A-600 states that nodules are acceptable if the hole diameter is above the minimum specified



Plating Voids

- Causes large stress concentrations & can result in crack initiation
- Location of the voids can provide crucial information in identifying the defective process
  - Around the glass bundles
  - In the area of the resin
  - At the inner layer interconnects (aka, wedge voids)
  - Center or edges of the PTH

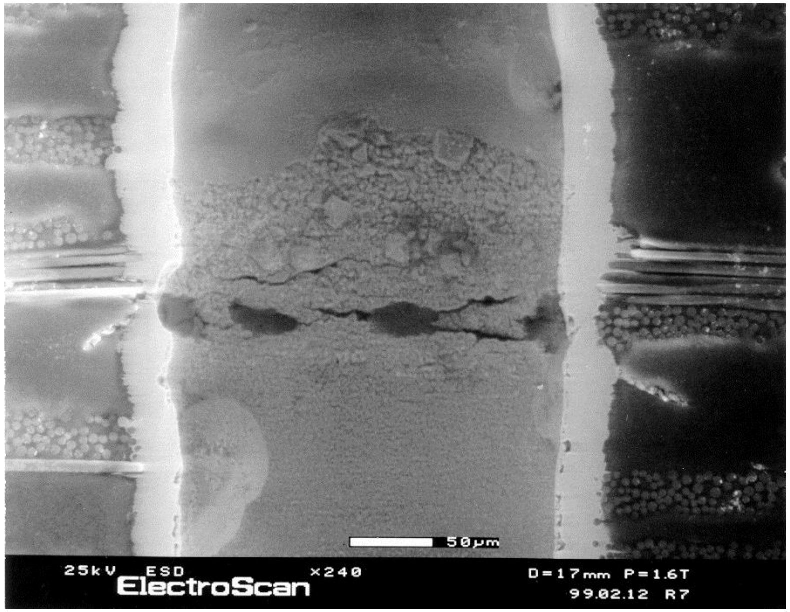


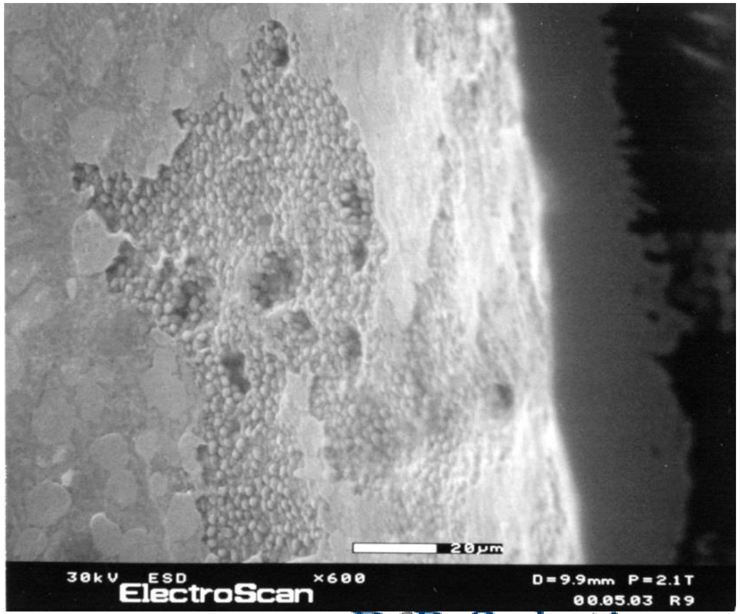


DfR Solutions

Etch Pits

- Occur due to either insufficient tin resist deposition or improper outerlayer etching process & rework
- Cause large stress concentrations locally
- Increases likelihood of crack initiation
- Large etch pits can result in a electrical open





How to Test & Qualify a Reliable PTV?

- There are currently six procedures for testing & qualifying a PTV
  - Modeling and simulation
  - Cross-sectioning + solder float/shock
  - Thermal shock testing (also thermal cycling)
  - Interconnect stress testing (IST)
  - Printed Board Process Capability, Quality, and Relative Reliability (PCQR2)
  - Highly Accelerated Thermal Shock (HATS)

Test & Qualify PTV

- Qualifying PTV is a two-step process

- The first step is to qualify the design and the PCB manufacturer
  - Initial qualification

- The second step is to initiate ongoing testing to monitor outgoing quality
  - Lot qualification

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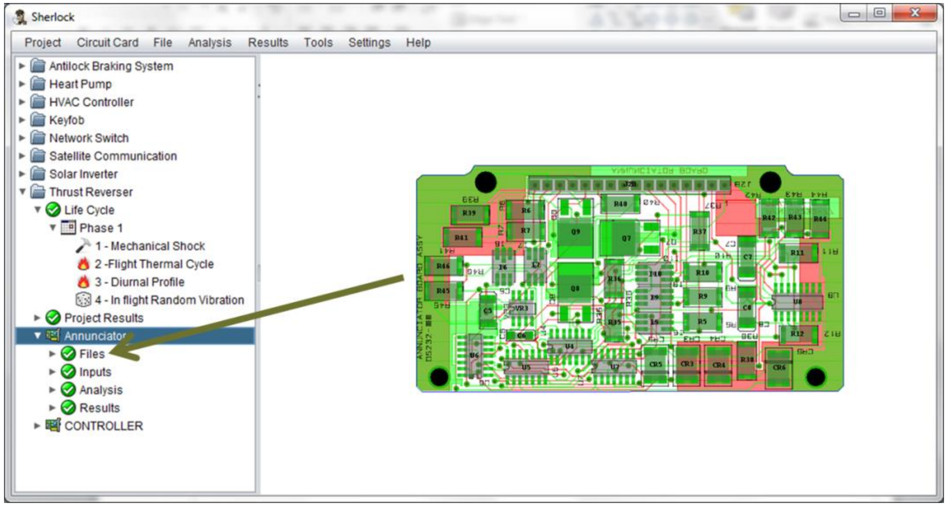
Initial Qualification

- Qualify the design through simulation / modeling
- DfR has implemented IPC TR-579 into Automated Design Analysis software, Sherlock, to allow for rapid assessment of PTV robustness
- First step: Define the environment (test or field or both)

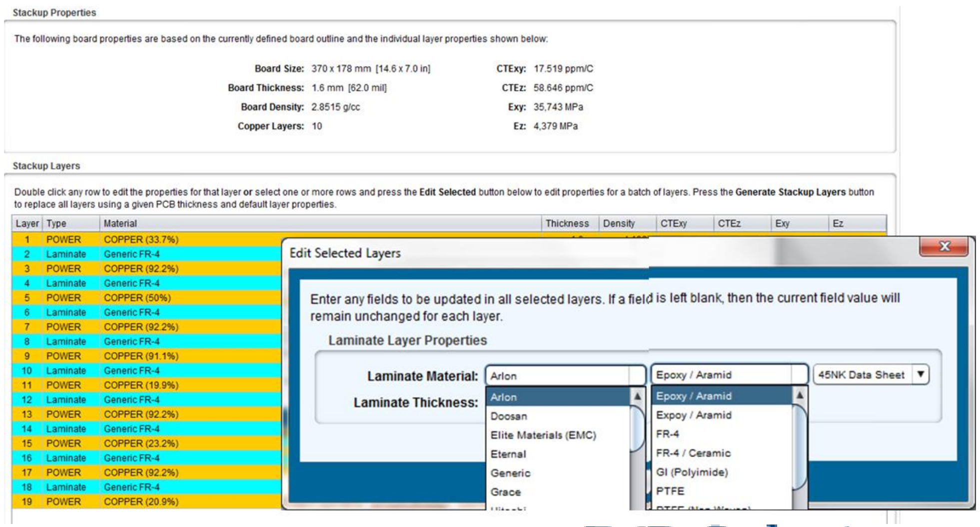
DfR Solutions

Simulation and Modeling

- <u>Second step</u>: Upload design information
  - Include thermal maps, if appropriate



- <u>Third step</u>: Select the laminate and prepreg material
  - Stackup and copper percentage automatically identified



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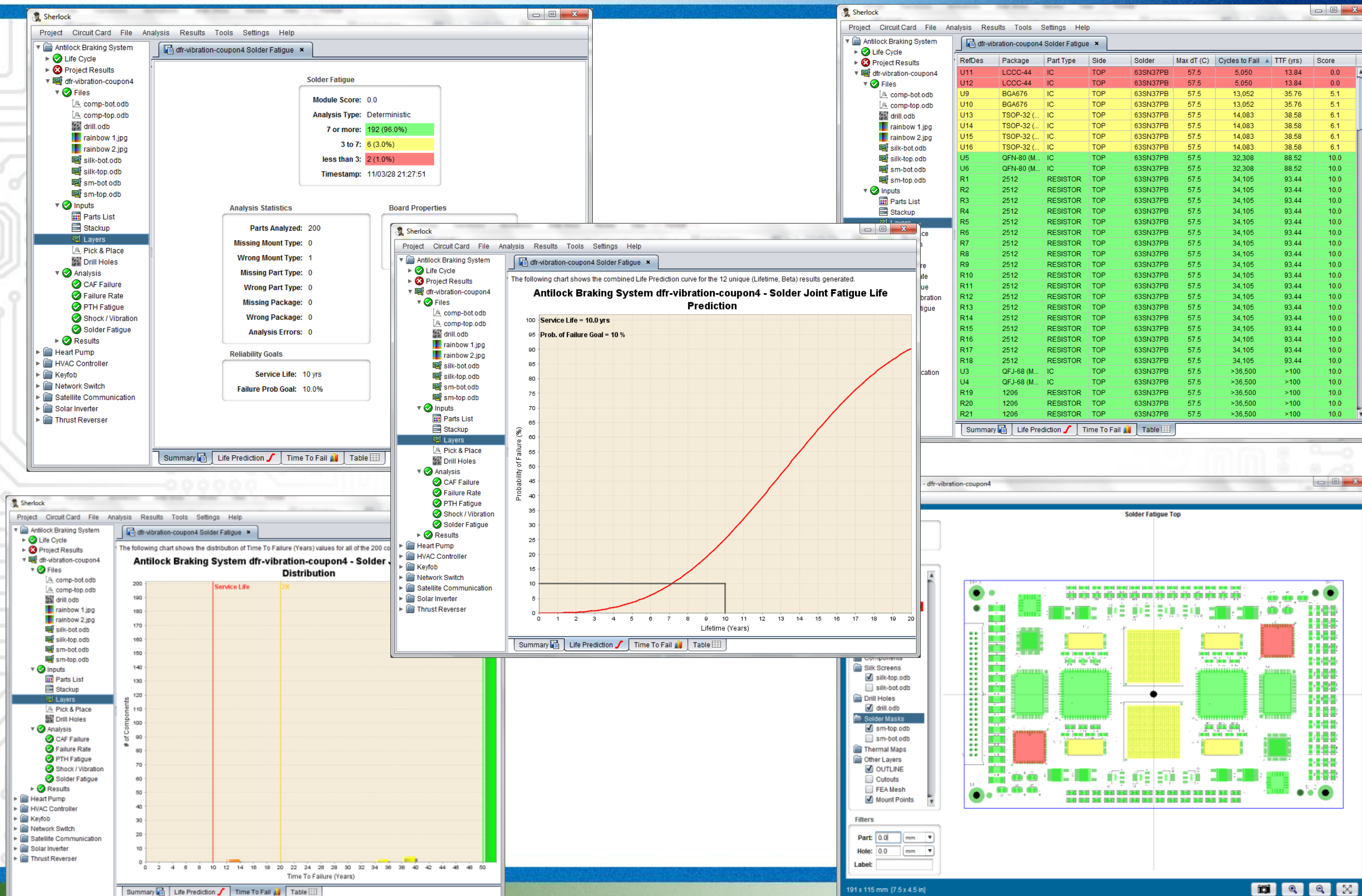
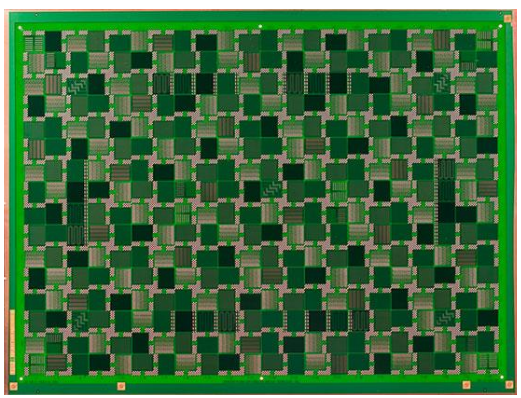
Results: Five Different Outputs



Initial Qualification (PCQR^2)

- Qualify the design and manufacturer through PCQR^2
  - Consists of a coupon design, a test standard, and a database
  - 18″ x 24″ layout with 1″ x 1″ test modules (352)
  - 2 – 24 layers (rigid, rigid-flex)
  - Three panels / three non-consecutive lots
  - Simulated assembly (6X) and thermal cycling (HATS)



Test Module	Design Type	Capability Information	Quality Information
Conductor/Space	Outerlayer, 0.5-oz. innerlayer, 1-oz. innerlayer, and buried-core	Conductor and space defect density	Conductor width and height uniformity
Via Registration	Through, 1-deep blind, 2-deep blind, controlled-depth drill, and back-drill	Via probability of breakout	
Via Formation	Through, 1-deep blind, 2-deep blind, buried-core, controlled-depth drill, and back-drill	Via defect densit	Via net resistance coefficient of variation
Via Reliability	Through, 1-deep blind, 2-deep blind, buried-core, controlled-depth drill, and back-drill	Yield loss	Percent change in resistance
Drill Overshoot	Controlled-depth drill	Probability of overshoot	
Drill Depth	Back-drill	Secondary drill depth	
Soldermask Registration	Outerlayer	Clearance yield	
Controlled Impedance	Single-ended and differential	Impedance uniformity	

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PCQR^2 (cont.)

- Advantages
  - Industry standard (IPC-9151)
  - Plug and play
  - Provides real data for understanding of PCB supplier capabilities and comparison to the rest of the industry through the use of an anonymous database
- Disadvantages
  - Industry-certified single source
  - $2K - $5K, not including panel costs

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Lot Qualification

- Interconnect stress testing (IST) is the overwhelming favorite of high reliability organizations
  - Small (1 x 4) coupon can fit along the edge of the panel
  - Testing is automated
  - Widely used
  - Ability to drive barrel fatigue and post separation
- Large number of holes (up to 300) and continuous resistance monitoring makes it far superior to cross-sectioning
  - And it should be cheaper!

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IST – Issues / Awareness

- Coupon design is critical (IST can be prone to problems)
- Need to specify preconditioning (IST or real reflow oven?)
- Need to specify frequency (every lot, every month, every quarter)
- Need to specify maximum temperature (some debate on the validity of results when above the Tg)
  - 130, 150, and 175C are the most common
- Need to specify requirements
  - Different markets/organizations specify different times to failure (300, 500, and 1000 cycles are most common)

Reliable PTV Summary

- The base knowledge and understanding of PTV Fatigue is robust
  - Decades of testing and simulation
  - Use of reliability physics is best practice
- Detailed understanding is still missing
  - Key expertise (process parameters, material properties, simulation, testing) is rarely in the same organization
  - Not a pure science activity (significant amount of human influence)
- Improvements in out-of-plane CTE and plating properties have greatly improved PTV performance
  - Avoiding defects continues to be the biggest risk

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Contamination and Cleanliness

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Why Contamination and Cleanliness?

- Believed to be one of the primary drivers of field issues in electronics today
  - Induces corrosion and metal migration (electrochemical migration – ECM)
- Intermittent behavior lends itself to no-fault-found (NFF) returns
  - Driven by self-healing behavior
  - Difficult to diagnose
- Pervasive
  - Failure modes observed on batteries, LCDs, PCBAs, wiring, switches, etc.
- Will continue to get worse as geometries shrink

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Failure Mode

- Why do you care about excessive contamination or insufficient cleanliness lead to?

Electro<u>chemical</u> Migration

(note: not Electromigration; completely different mechanism)

- Understanding the mechanism provides insight into the drivers and appropriate mitigations

What is ECM?

- Definition
  - Movement of metal through an electrolytic solution under an applied electric field between insulated conductors
- Electrochemical migration can occur on or in almost all electronic packaging
  - Die surface
  - Epoxy encapsulant
  - Printed board
  - Passive components
  - Etc.

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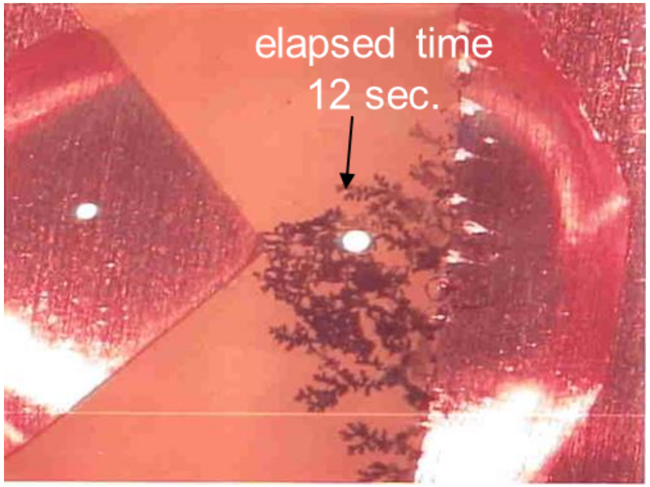
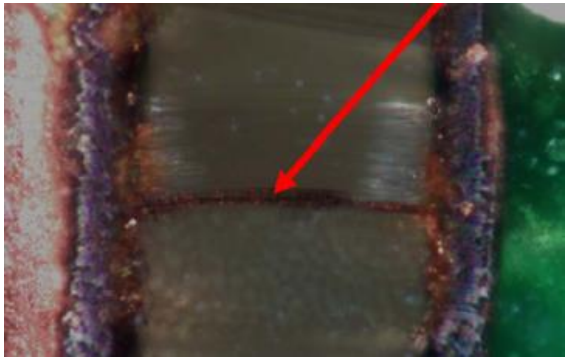
ECM Mechanisms

- Some ECM Mechanisms have more definitive descriptions

- Dendritic growth
  - Descriptor for ECM along a surface that produces a dendrite morphology
  - “Tree-like”, “Feather-like”



- Conductive anodic filaments (CAF)
  - Descriptor for migration within a printed circuit board (PCB)



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ECM Steps

- Traditional electrochemical migration involves four steps
  - Path formation
  - Electrodissolution
  - Ion migration
  - Electrodeposition
- In ECM along internal surfaces (e.g., CAF), ion migration / electrodeposition ‘co-exist’

Path Formation

- Physio-chemical changes necessary to initiate ECM
  - Different meanings for different mechanisms
  - Believed to be the rate-limiting step
- Dendritic growth
  - The creation of an electrolytic solution sufficiently conductive
  - Driven by relative humidity, contaminants, delamination
- Conductive anodic filaments (CAF)
  - Degradation of the epoxy/glass interface

Contamination

- Two concerns
  - Hygroscopic contaminants
  - Ionisable contaminants that are soluble in water (e.g., acids, salts)
- Ionic contaminants of greatest concern
  - Primarily anions; especially halides (chlorides and bromides)
    - Very common in electronics manufacturing process
    - Silver(I) ions are soluble at higher pH; reason it is one of easiest to form dendrites.
  - Cations primarily assist in the identifying the source of anions
    - Example: Cl with K suggests KCl (salt from human sweat)

Sources of Contaminants

- Printed board fabrication process
  - Insufficiently cured polymers
- Rinse water
- Fluxes
- Handling
- Storage and use environment

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Sources of Contaminants (cont.)

Ion	Possible Sources
Cl	Board Fab, Solder Flux, Rinse Water, Handling
Br	Printed Board (flame retardants), HASL Flux
Fl	Teflon, Kapton
PO_4	Cleaners, Red Phosphorus
SO_4	Rinse Water, Air Pollution, Papers/ Plastics
NO_4	Rinse Water
Weak Organic Acids	Solder Flux

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Printed Board Fabrication Process

- One of the most common source of contaminants
  - Greatest use of active/aggressive chemicals
  - Low margin business
  - Increasing use of no-clean assembly process
    - Last chance to clean

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PCB Contaminants (examples)

- Etching
  - Chloride-based: Alkaline ammonia (ammonium chloride), cupric chloride, ferric chloride, persulfates (sometimes formulated with mercuric chloride)
  - Other: Peroxide-sulfuric acid
- Neutralizer
  - Hydrochloric acid
- Cleaning and degreasing
  - Hydrochloric acid, chlorinated solvents (rare)
- Photoresist stripping
  - methylene chloride as a solvent
- Oxide
  - Sodium chlorite
- Electroless plating
  - Sodium hypochlorite (in potassium permanganate)
  - Palladium chlorides (catalyst)

Printed Board Fab (other examples)

- Bromide sources
  - Surface processes
    - Solder masks, marking inks, and fluxes
  - Flame retardant
    - FR-4 Epoxy has used a brominated bisphenol A (TBBA) epoxy resin
    - IPC-TR-476A: "Bromide in epoxy resin can diffuse to the surface during a high temperature process such as soldering"
  - Halogen-free laminates increasingly available

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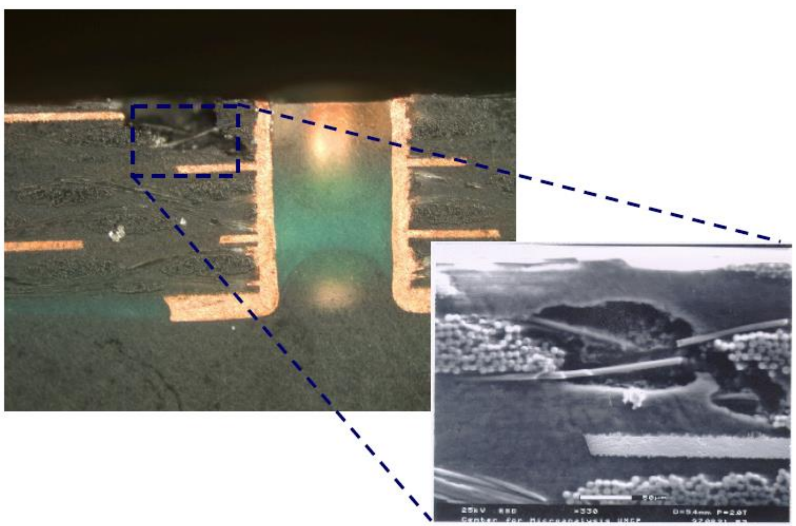
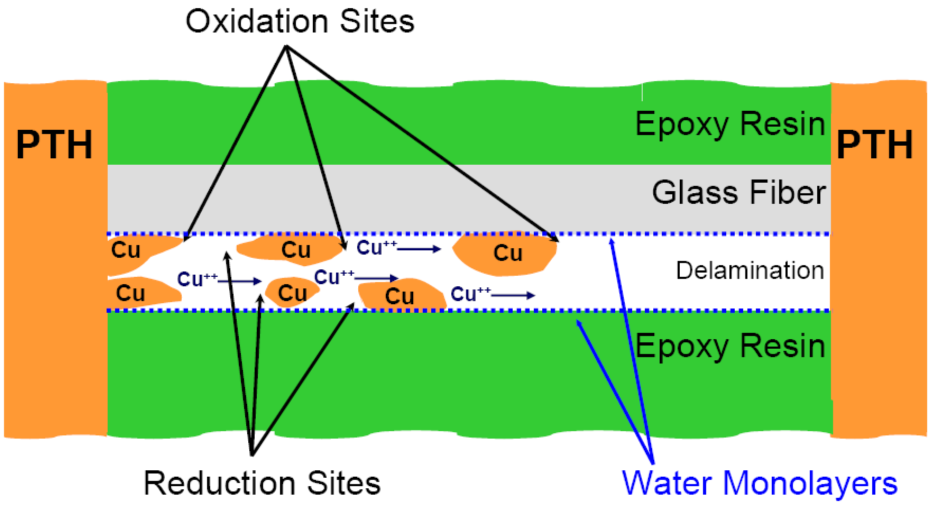
Insulation

- The influence of insulation (migration surface) on ECM is poorly quantified
- Hydrophobic surfaces superior
  - Silicone
- Solder mask / FR4 epoxy selection rarely based on ability to resist ECM
  - Exposed epoxy glass is much more hydrophilic than most solder mask materials
- Greater concern and investigation with CAF
  - Degradation of insulation (epoxy/glass interface) results in path formation

PCB Conductive Anodic Filaments (CAF)

- CAF also referred to as metallic electro-migration
- Electro-chemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field
- CAF can cause current leakage, intermittent electrical shorts, and dielectric breakdown between conductors in printed wiring boards





CAF: Examples

Influenced by electric field strength, temperature, humidity, laminate material, soldering temperatures, and the presence of PCB manufacturing defects.

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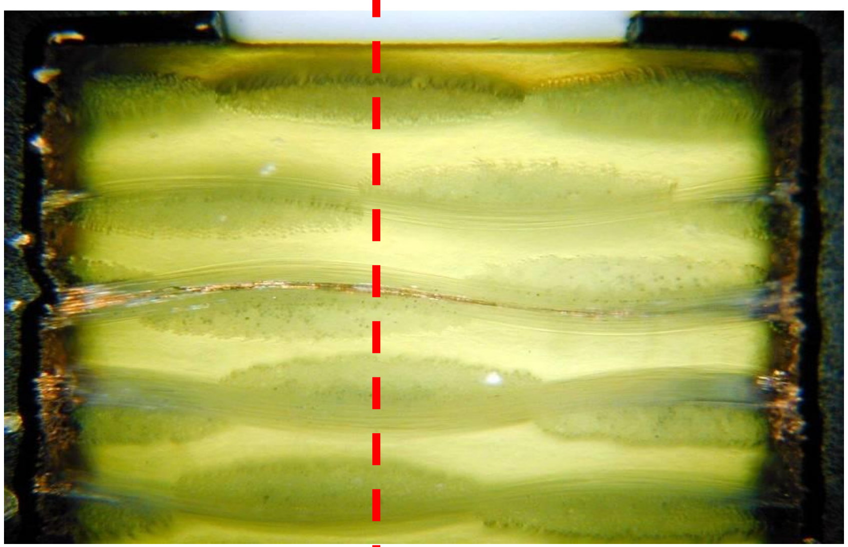

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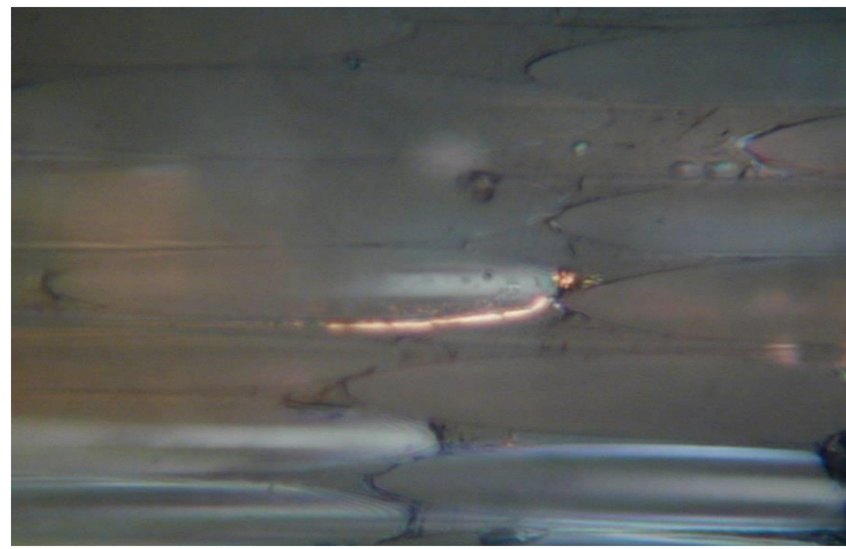

A:A Cross-Section

Request a CAF-resistant laminate and monitor PCB supplier plating & drilling processes!

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reliability designed, reliability delivered

Ion Chromatography, Cleanliness & IPC Standards

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IPC PCB Cleanliness Standards

- IPC-5701: Users Guide for Cleanliness of Unpopulated Printed Boards
- IPC-5702: Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards
- IPC-5703: Guidelines for Printed Board Fabricators in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards
- IPC-5704: Cleanliness Requirements for Unpopulated Printed Boards

IPC PCB Cleanliness Standards

- IPC-6012B, Qualification and Performance Specification for Rigid Printed Boards, Section 3.9
  - Requires confirmation of board cleanliness before solder resist application
  - *When specified*, requires confirmation of board cleanliness after solder resist or solderability plating
- Board cleanliness before solder resist shall not be greater than 10 ug/in^2 of NaCl equivalent (total ionics)
  - Based on military specifications from >30 years ago
- Board cleanliness after solder resist shall meet the requirements specified by the customer

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Cleanliness Control: Test Procedures

- IPC-6012B specifies a Resistance of Solvent Extract (ROSE) method
  - Defined by IPC-TM-650 2.3.25
- IPC-6012B specifies this measurement should be performed on production boards every lot
  - Class 1 boards: Sampling Plan 6.5
  - Class 2 and 3 boards: Sample Plan 4.0
- Sampling plan (example)
  - If a lot contains 500 panels of a Class 2 product, 11 panels should be subjected to ROSE measurements for cleanliness testing

IPC Ionic Contamination Test Standards

- Resistivity of Solvent Extract (ROSE) Test Method IPC-TM-650 2.3.25
  - **Bare PCBs**
  - The ROSE test method is used as a process control tool to detect the presence of bulk ionics. The IPC upper limit is set at 10.0 mg/NaCl/in2. This test is performed using a Zero-Ion or similar style ionic testing unit that detects total ionic contamination, but does not identify specific ions present. This process draws the ions present on the PCB into the solvent solution. The results are reported as bulk ions present on the PCB per square inch.
- Modified Resistivity of Solvent Extract (Modified ROSE) Test Method TM 2.3.25.1
  - The modified ROSE test method involves a thermal extraction. The PCB is exposed in a solvent solution at an elevated temperature for a specified time period. This process draws the ions present on the PCB into the solvent solution. The solution is tested using an Ionograph-style test unit. The results are reported as bulk ions present on the PCB per square inch.
- Ion Chromatography IPC-TM-650 2.3.28.2
  - **Bare PCBs**
- Ion Chromatography IPC-TM-650 2.3.28
  - **Populated PCBs**
  - This test method involves a thermal extraction similar to the modified ROSE test. After thermal extraction, the solution is tested using various standards in an ion chromatograph test unit. The results indicate the individual ionic species present and the level of each ion species per square inch.

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Test Procedures: Common Problems

- ROSE is the least sensitive of ionic measurement techniques
  - 5 ug/in^2 detected by ROSE is equivalent to ~20 ug/in^2 detected by ion chromatography
- Equipment is not calibrated
- Insufficient volume of solution is used
- Insufficient surface area
  - Panels are preferred over single boards
- Cut-outs are not considered when calculating surface area
- Insufficient measurement time
  - 7 to 10 minutes is preferred

Technique	Technology	Equivalency Factor
ROSE	Static / Unheated	1
Omega-Meter	Static / Heated	~1.5
Ionograph	Dynamic / Heated	~2.0
Modified-ROSE, Zero-Ion, etc.	Varied	~4.0 (?)
Ion Chromatography	80C for 1 hr	~4.0

Test Procedures: Best Practice

- Ion Chromatography (IC) is the 'gold standard'
  - Some, but very few, PCB manufacturers qualify lots based on IC results

- Larger group uses IC to baseline ROSE / Omegameter / Ionograph (R/O/I) results
  - Perform lot qualification with R/O/I
  - Periodically recalibrate with IC (every week, month, or quarter)

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How to Measure Cleanliness Using Ion Chromatography

- Standard ion chromatography (IC) testing
  - IPC-TM-650, Method 2.3.28A
  - Submerge whole board; 75 IPA / 25 DI
- Updated IC
  - IPC-TM-650, Method 2.3.28.2
  - Submerge whole board; 10 IPA / 90 DI (Delphi requirements)
- Modified IC
  - Use of saponifiers or alternative solvent
  - Submerge whole board
- Localized Testing
  - C3 from Foresite

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Cleanliness Control: Requirements

- The majority of knowledgeable OEMs completely ignore IPC cleanliness requirements
- Option 1: Requirements are based on R/O/I test results, but adjusted for lack of sensitivity
  - Most companies now specify 2.5 to 7 ug/in^2
- Option 2: Requirements are based on IC test results and then monitored using R/O/I

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Hygroscopic Residues

- Certain contaminants create conditions that increase moisture film thickness
  - Increase risk of condensation
  - Ionic and non-ionic contaminants
- Examples: Polyglycols
  - When present, turns surface from hydrophobic (water repelling) to hydrophilic (water attracting)
  - Non-ionic: Not detectable using ion chromatography or Omegameter

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Major Appliance Manufacturer (IC)

Contaminant	Incoming PCB	Processed PCB	
	Maximum Level (ug/in^2)	Maximum Level (ug/in^2)	Upper Control Limit (ug/in^2)
Ammonium	<0.5		<2
Bromide	3	10	8
Calcium	<0.5		<1
Chloride	2.5	3.5	3
Fluoride	<0.5		<1
Magnesium	<0.5		<1
Nitrate	<0.5		<2
Nitrite	<0.5		<1
Phosphate	<0.5		<1
Potassium	<3		<3
Sodium	<3		<3
Sulfate	3	3	2
Total	5	18	14
Weak Organic Compounds	200	200	50

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PCB Cleaning: Process Flow

- At a minimum, PCB manufacturers should clean the PCB:
  - Immediately before the application of solder resist
  - Immediately after the application of any solderability plating
    - HASL
    - Electroless Nickel and Immersion Gold
    - Immersion Tin
    - Immersion Silver
- Some PCB manufacturers also perform a final clean
  - Should not substitute for cleaning after solderability plating
  - Residues from plating operations can become more difficult to remove with any time delay

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PCB Cleaning Process: Requirements

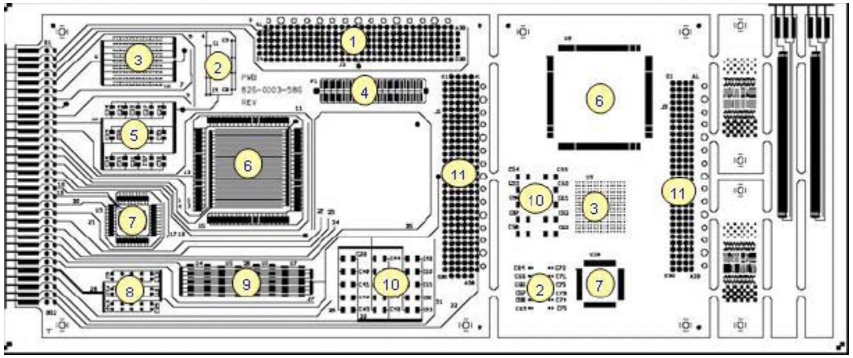
- Final rinse with deionized (DI) water
  - 2-8 MΩ is preferred; >10 MΩ may be too aggressive
  - Distilled water is insufficient
  - ‘City’ water is unacceptable
- Potential options
  - Use of saponifier during the cleaning process
  - Heated DI water is nice, but not absolutely necessary
- Common problems
  - DI water is only used if specified by the customer
  - DI water is turned off to reduce water and energy usage
  - Failure to monitor DI water at the source
  - Failure to alarm the DI water on the manufacturing floor

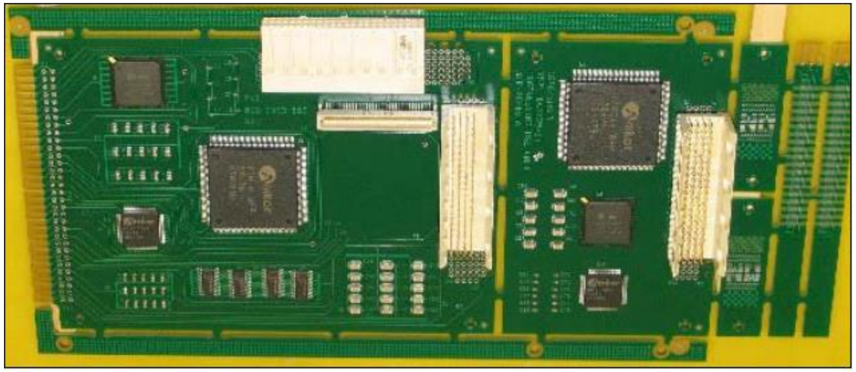
Process Material Qualification – SIR Recommendation

- Validate compatibility and performance of all new process materials using SIR testing
  - IPC-B-52 SIR TEST VEHICLE
  - IPC-A-52:Cleanliness and Residue Evaluation Test Board – Single User CD-ROM
    - The IPC-B-52 test board is intended to be a process qualification vehicle, with the materials of construction and source of test boards to be representative
    - https://portal.ipc.org/Purchase/ProductDetail.aspx?Product_code=5e7a8626-b486-db11-a4eb-005056875b22

IPC-B-52 (IEC TB-57)

- The latest generation of test coupons
- Similar to designs from NPL, Rockwell Collins, & IBM
  - Main SIR Test Board
  - IC Test Coupon
  - Solder Mask Adhesion
  - SIR mini-coupons
- Packages
  - 0402 – 1206
  - QFP (no 0.4mm pitch)
  - SOICs and BGAs
  - Through-Hole Header
  - Comb patterns (5 mil)





Not specifically called out in any TM-650 test method

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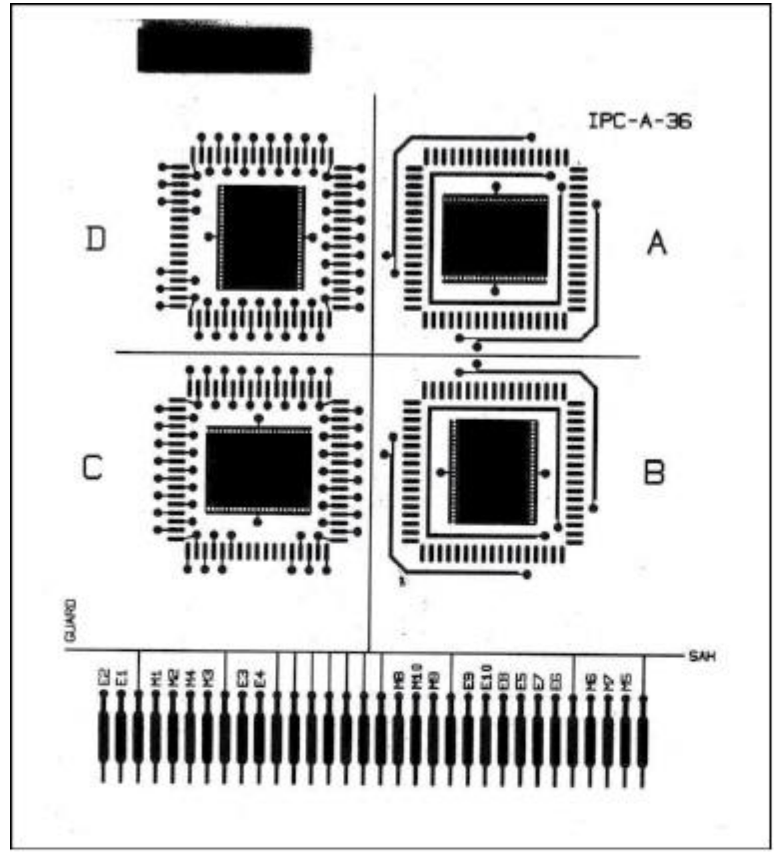
IPC A-36D, IPC B-36

- IPC A-36D: Cleaning Alternatives Artwork - IPC-D-350 Format
- Used in cleaning studies
- 4 quadrants utilizing both surface mount patterns and vias
  - Each with 68 I/O chip carrier sites and 10 SIR test points



Recommended Test Method

- Flux application and preconditioning
  - Solder paste
  - Wave solder
  - Rework
- Exposure to low temperature and maximum humidity without condensation
  - 35 to 40C
  - Minimum of 93%RH
  - 72 to 120 hours of exposure
  - Continuous monitoring (1 second per reading)

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Product Qualification

- Consider testing entire product, if resource or time limited
  - 40C/93%RH for 72 to 120 hours
  - Extend time period of using conformal coating or potting material
- Do not test at 85C/85%RH for dendritic growth (surface ECM)
  - Some issues with conductive anodic filament (CAF) as well
- Study by Sohm and Ray (Bell Labs) demonstrated degradation of weak organic acid residues above ~55C
  - Reduces their effect on surface insulation resistance
- Turbini demonstrated breakdown of polyglycols at elevated temperature as well
  - Absorption into board can increase risk of CAF

Conclusion

- Contamination and Cleanliness requirements should be clearly detailed to the supply chain
- Cleanliness should be validated
  - Materials compatibility (test coupon)
  - Product qualification
  - Ongoing cleanliness assessment (IC)

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Considerations for Selecting a PCB Surface Finish

Importance of SF

- The selection of the surface finish on your PCBs could be the most important material decision made for the electronic assembly.
- The surface finish influences the process yield, the amount of rework, field failure rate, the ability to test, the scrap rate, and of course the cost.
- One can be lead astray by selecting the lowest cost surface finish only to find that the eventual total cost is much higher.
- The selection of a surface finish should be done with a holistic approach that considers all important aspects of the assembly.

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Surface Finishes - Post Pb-Free

- Multiple Pb-Free Surface Finish Options Now Exist
  - No clear winner, no ideal solution

- Each PCB surface has different advantages and disadvantages that affects fabrication, solderability, testability, reliability, or shelf life

- The 5 most popular Pb-Free Surface Finishes are:
  - Electroless nickel/immersion gold (ENIG)
    - And ENEPIG (electroless Pd added)
  - Immersion silver (ImAg)
  - Immersion tin (ImSn)
  - Organic solderability preservative (OSP)
  - Pb-free HASL.
- These finishes (except for Pb-free HASL) have been in use for several years.
- Newer finishes are currently being developed (direct Pd, PTFE-like coatings, nanofinishes)

What is your SF selection approach?

- **Component Procurement:** Select the cheapest one and let the engineers figure out how to use it.
- **PCB Engineer:** Select the finish that is easiest for the suppliers to provide (their sweet spot); let the assembler figure out how to use it.
- **Assembly Engineer:** Select the finish that provides the largest process window for assembly and test.
- **Sustaining Engineer:** Select the finish that minimizes field failures.
- **CEO:** Select the finish that minimizes the overall cost (including reliability risk).

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Considerations with SF Selection

- Cost sensitivity
- Volume of product (finish availability)
- SnPb or LF process
- Shock/Drop a concern?
- High yield ICT is important
- Is direct wire bonding required?
- User environment (corrosion a concern)?
- Fine pitch assembly (<0.5 mm)
- Wave solder required (PCB > 0.062")
- Are cosmetics of the PCB a concern?

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Surface Finish Selection Guideline

Attributes

Cost Sensitive Product

High Volume Required

Cosmetics of Finish is Important

High Yield ICT Required

SF Type

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

Wire bonding to Finish is Required

Capable

Not Capable

Surface Finish Selection Guideline

Attributes

Cost Sensitive Product

High Volume Required

Cosmetics of Finish is Important

High Yield ICT Required

OSP

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

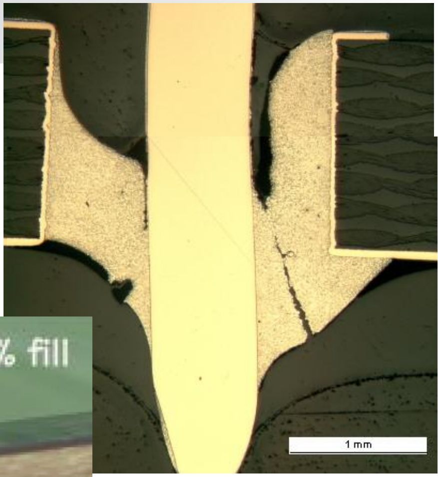
Wire bonding to Finish is Required

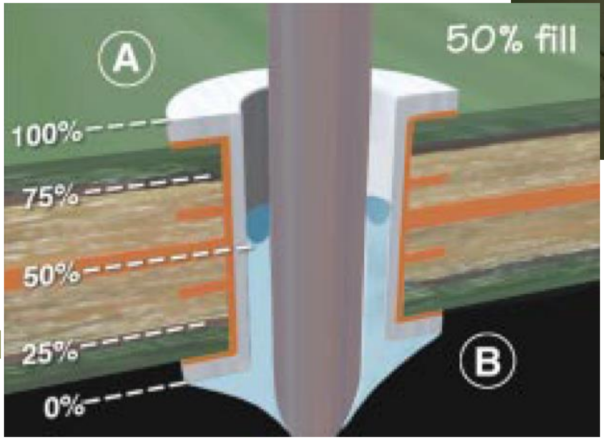
Capable

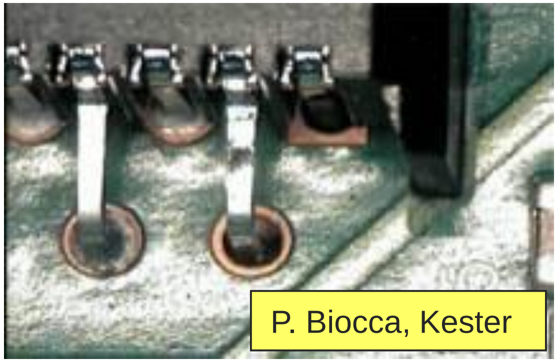
Not Capable

OSP Issues: Plated Through-Hole Fill

- Solder fill is driven by capillary action
- Important parameters
  - Hole diameter, hole aspect ratio, wetting force
  - Solder will only fill as long as its molten (key point)
- OSP has lower wetting force
  - Risk of insufficient hole fill
  - Can lead to single-sided architectu
- Solutions:
  - Changing board solderability plating
  - Increasing top-side preheat
  - Increasing solder pot temperature (some go as high as 280ºC)
    - Not recommended!
  - Changing your wave solder alloy

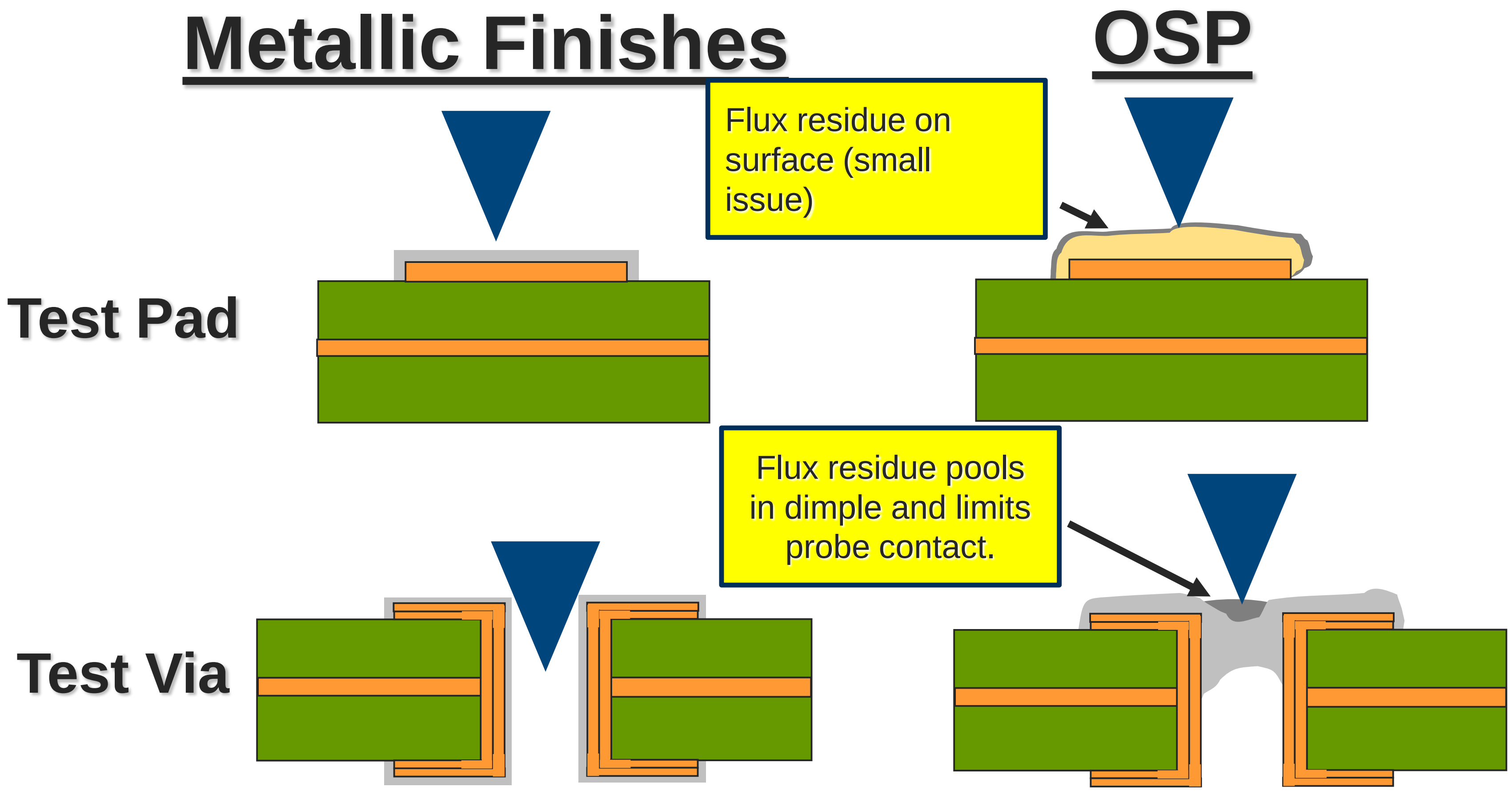






In Circuit Test w/ OSP – test via challenges

- Probing through HT OSP is not recommended.
- Solder paste is printed over OSP test pads/vias (leaving flux residue with no-clean paste).`



Space constraints on PCB make it difficult to eliminate test vias.

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Surface Finish Selection Guideline

Product Attributes

ImAg

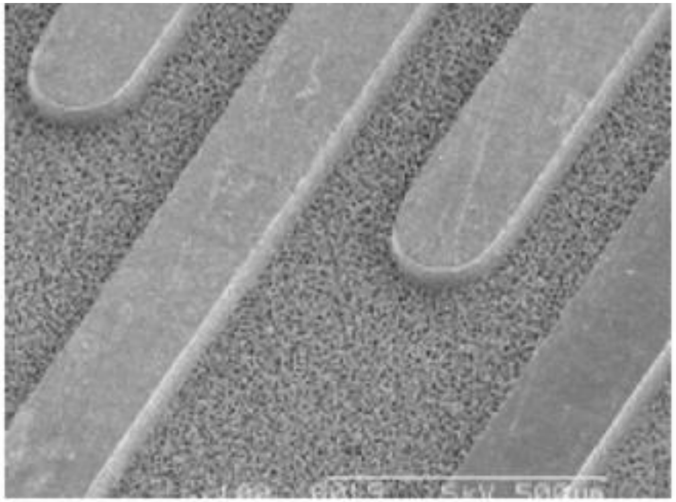
- Cost Sensitive Product
- High Volume Required
- Cosmetics of Finish is Important
- High Yield ICT Required
- Pb-Free Wave Solder (PCB > 62mil)
- Pb-Free Shock/Drop is a Concern
- Fine Pitch Components Used
- Corrosion Failure is Possible
- Wire bonding to Finish is Required

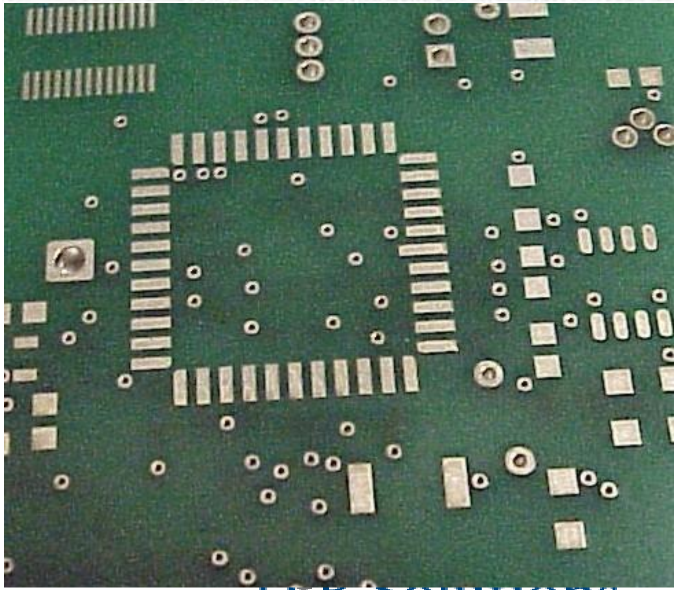
Capable

Not Capable

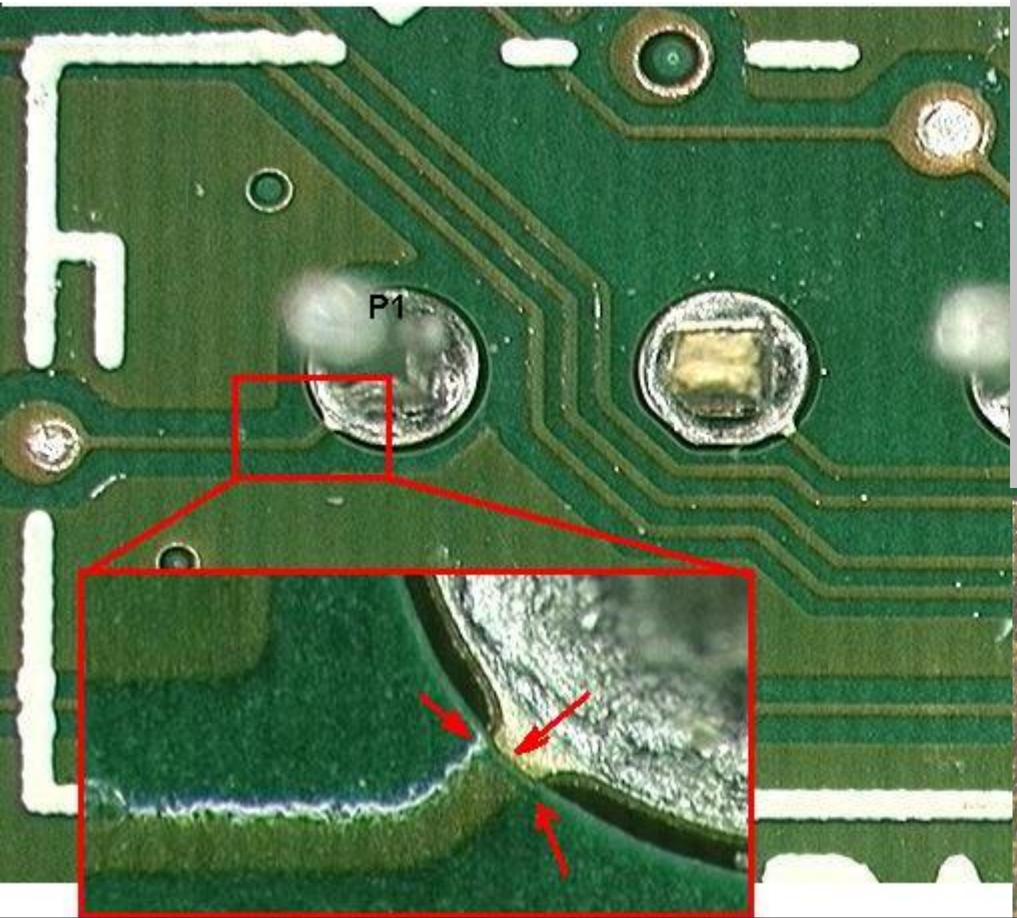
Immersion Silver Ag (ImAg)

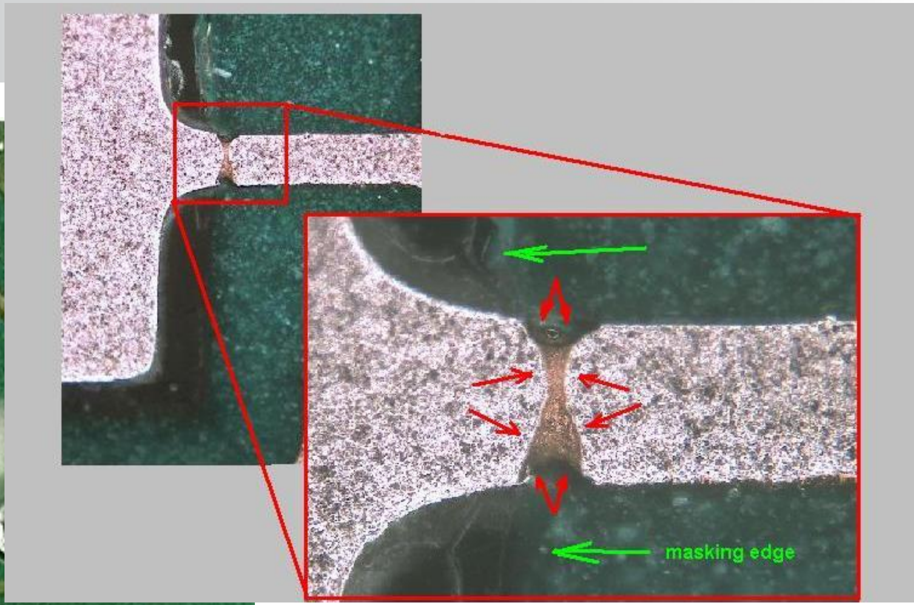
- Single material system
  - Specified by IPC-4553
- Thickness is typically 6-20 u”
- Benefits
  - Good flatness & coplanarity
  - Good shelf life if packaged properly.
  - Good oxidation resistance & shelf life.
  - Good wettability and reflow performance.
  - Good testability
  - Low cost

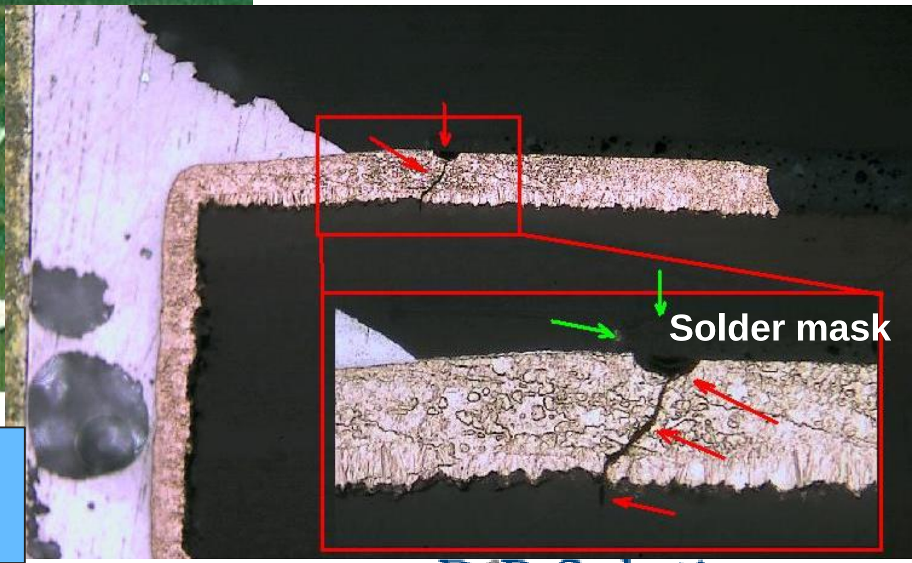




ImAg Trace Etching

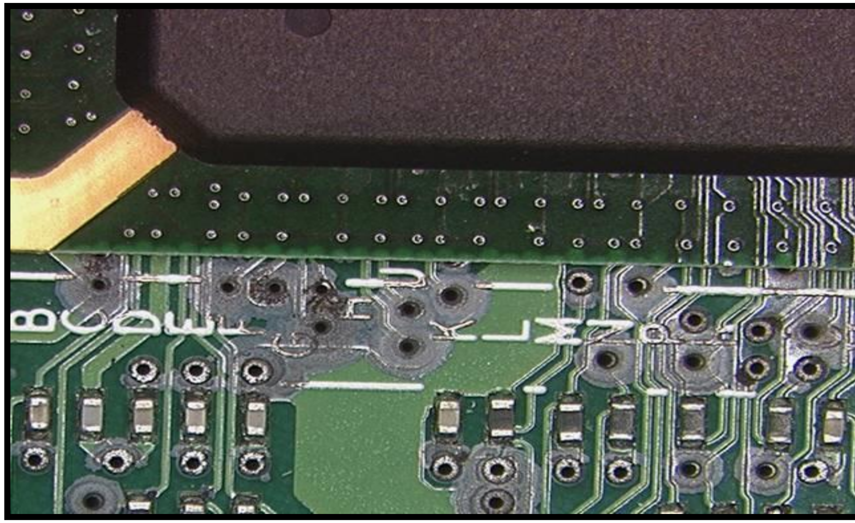




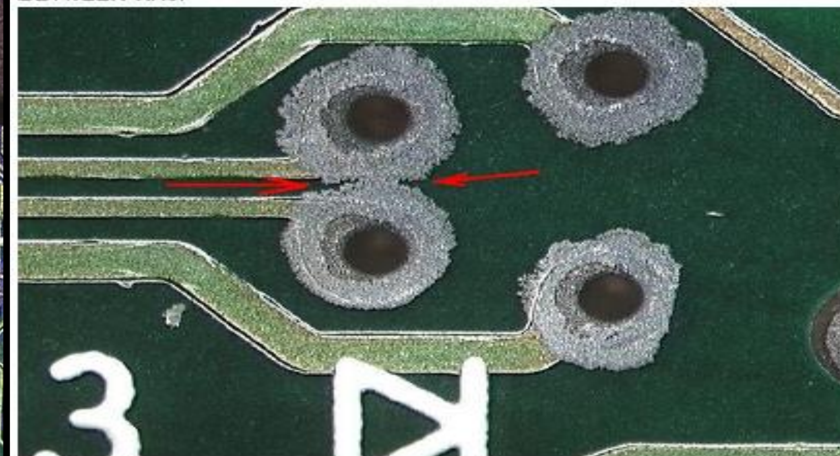


Galvanic etching can occur SM edge if PCB rinsing and drying not adequately performed.

Creep Corrosion



PICTURE 3361_1a1 SHOWING A CLOSE-UP OF THE BRIDGING GROWTH BETWEEN VIAS.



- Corrosion product is poorly conductive (resistance of about 1Mohm).
- Conductivity is higher when the humidity is high.
- Field returns often function fine – since corrosion product has dried out.
- Features most sensitive to leakage current will trigger the system failure (failing symptoms can vary system-to-system).
- Visual inspection is often required to diagnose.

ImAg Creep Corrosion - Affected Locations

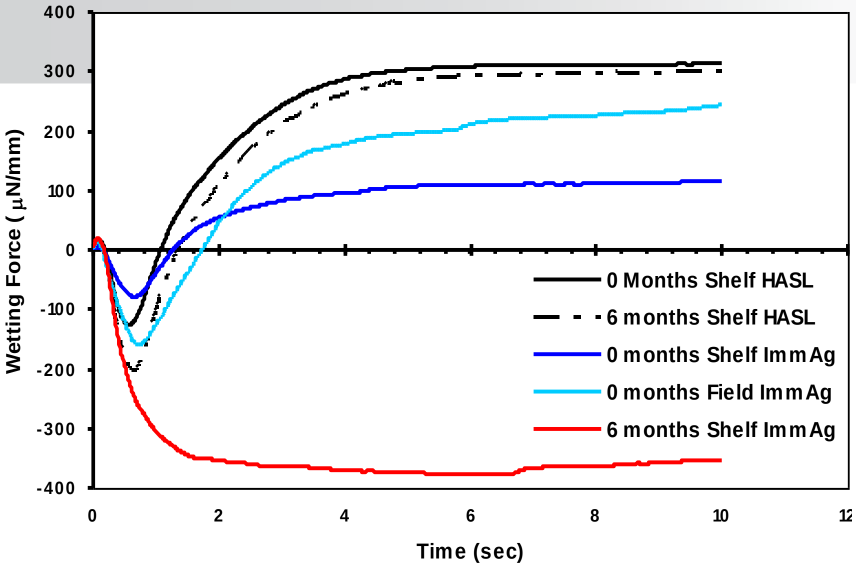
- Paper mills
- Rubber manufacturing (tires for example).
- Fertilizer
- Waste water treatment
- Mining/smelting
- Cement or asphalt production
- Petrochemical
- Clay modeling studios
- Regions of the world with poor air quality
- Etc. - includes companies nearby such industries

- Product is less impacted if airflow to PCBA is restricted.

DfR Solutions

Impact of Tarnish

- Shelf life can be an issue
  - If not stored in protective bags
  - Significant degradation when exposed to corrosive gases



- Tarnish after assembly is mostly cosmetic – but will impact perception of quality.
- If PCBA is visible to user tarnish may be an issue.
- Scrap costs may increase considerably if PCBAs are repaired and sent back into service.
  - Boards that appear black but are still functional are often thrown out.

Surface Finish Selection Guideline

Product Attributes

Cost Sensitive Product

High Volume Required

Cosmetics of Finish is Important

High Yield ICT Required

ImSn

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

Wire bonding to Finish is Required

Capable

Not Capable

Immersion Sn (ImSn)

- Single material system
  - Specified by IPC-4554
    - Standard thickness: 1 micron (40 microinches)
    - Some companies spec up to 1.5 microns (65 microinches)

- Benefits
  - Excellent flatness, low cost

- Not as popular a choice with PCB fabricators
  - Environmental and health concerns regarding thiourea (a known carcinogen)
  - Some concern regarding tin whiskering (minimal)

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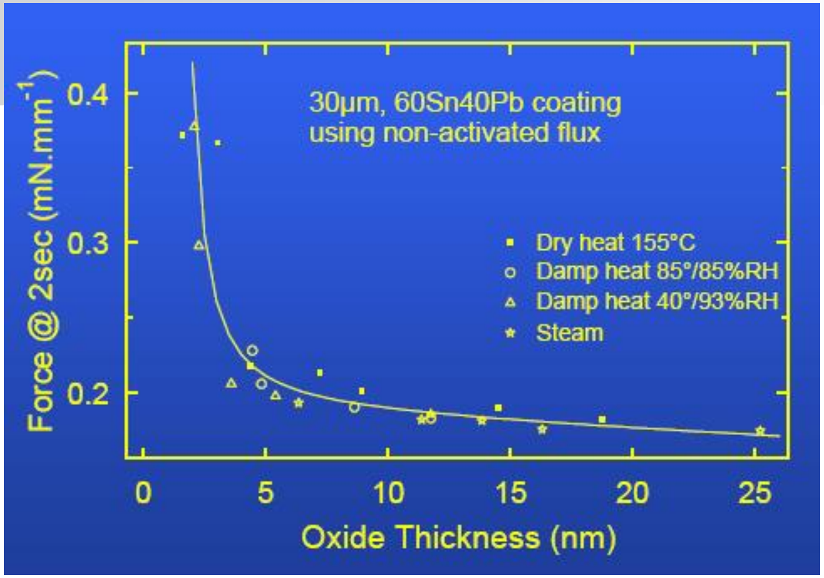
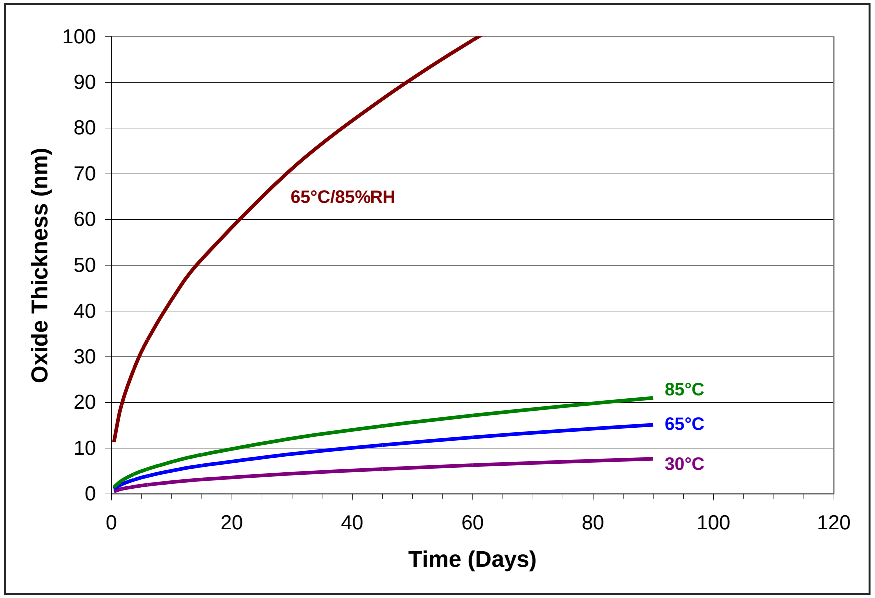
ImSn:Quality Issues & Failure Mechanisms

- Insufficient thickness.
  - **Decreases solderability during storage or after 2nd reflow – due to IMC growth through the thickness.**
- Solderability problems with oxide thickness greater than 5 nm
  - Excessive oxide thicknesses (50-100nm) periodically observed.
- Drivers of oxidation.
  - Exposure to humid conditions (>75%RH)
    - Greatly accelerates oxide growth through the creation of tin hydroxides.
      - Use sealed moisture/air tight wrapping for shipping and cool, low humidity storage
  - Cleanliness of the raw board.
    - Contaminates breaks down self-limiting nature of tin oxides
    - Accelerates oxide growth





DfR Solutions

Surface Finish Selection Guideline

Product Attributes

Cost Sensitive Product

High Volume Required

Cosmetics of Finish is Important

High Yield ICT Required

ENIG
ENEPIG

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

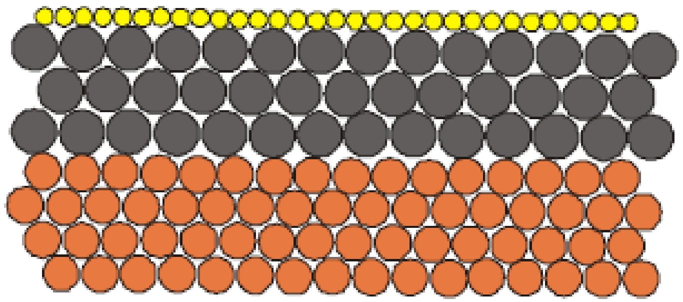
Wire bonding to Finish is Required

Capable

Not Capable

Electroless Nickel/Immersion Gold (ENIG)

- Two material system
  - Defined by IPC-4552 Specification for Electroless Nickel/Immersion Gold.
  - Electroless nickel.
    - 3 – 6 microns
  - Thin Immersion gold top coat
    - 0.08-0.23 microns



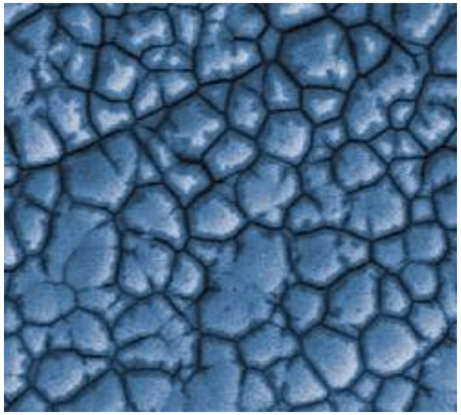
- Benefits
  - Excellent flatness and long-term storage
  - Excellent oxidation resistance and wetting properties
  - Robust for multiple reflow cycles
  - Supports alternate connections (wirebond, separable connector) & electrical testability.
  - Moderate costs.
  - Gold readily dissolves into solder and does not tarnish or oxidize making it an excellent choice for a surface finish.
    - But gold cannot be directly plated onto copper, since copper diffuses into gold, which allows the Cu to reach the surface and oxidize which reduces solderability.
    - Nickel is serves as a barrier layer to copper, the thin gold coating protects the nickel from oxidizing.

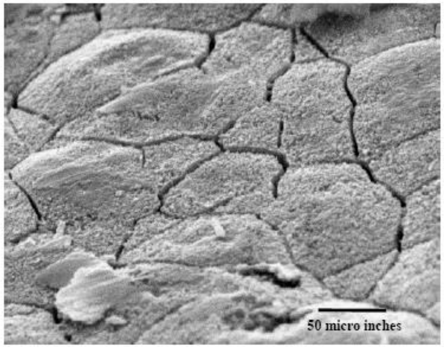
DfR Solutions

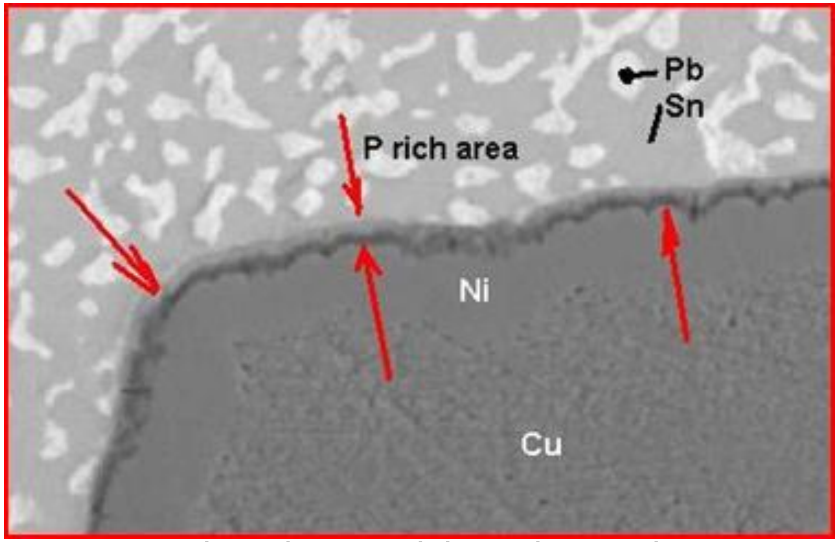
ENIG: Primary Reliability Risks

- Black pad drivers
  - Phosphorus content
    - High levels = weak, phosphorus-rich region after soldering
    - Low levels = hyper-corrosion (black pad) Insufficient Phosphorous will not prevent corrosion during the highly acidic immersion gold (IG) process
  - Cleaning parameters
  - Gold plating parameters
  - Bond pad designs
- Causes a drop in mechanical strength
  - Difficult to screen
  - Can be random (e.g., 1 pad out of 300)
- Ni-Sn intermetallic produces a brittle interface when used with SAC solder

Images of Black Pad

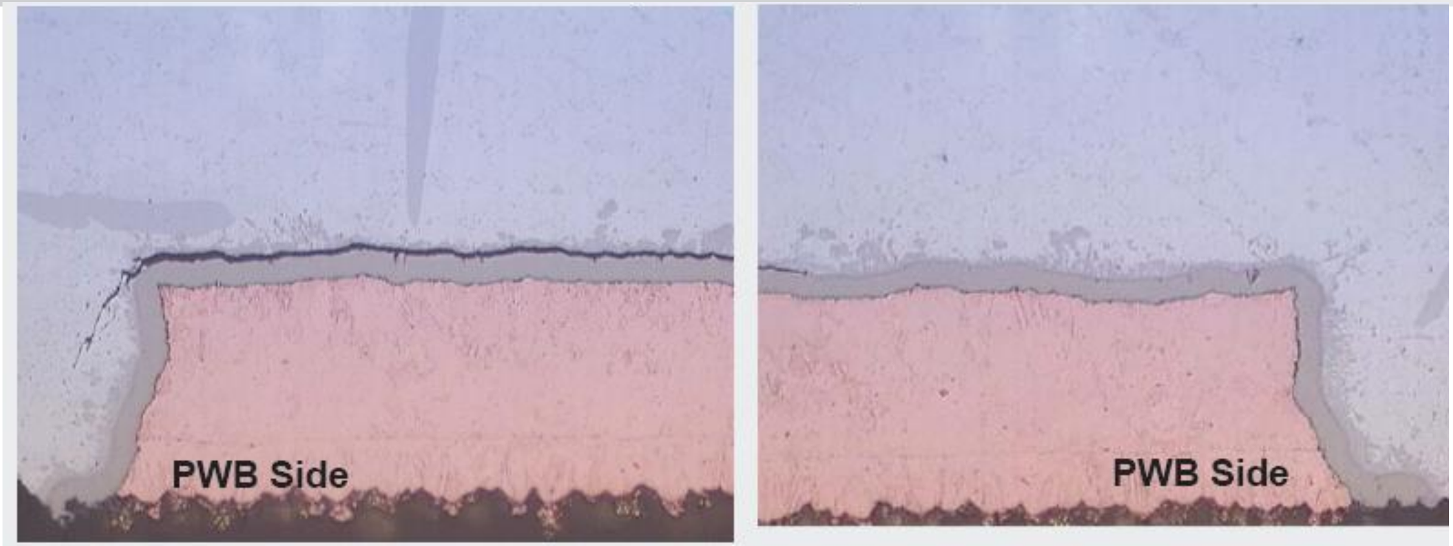






Phosphorus-Rich Dark Streak

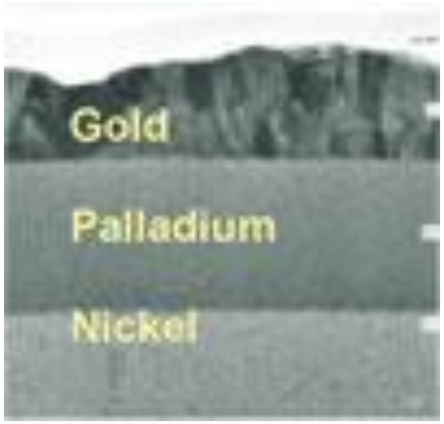
ENIG - Ni Interface Issues w/ SAC



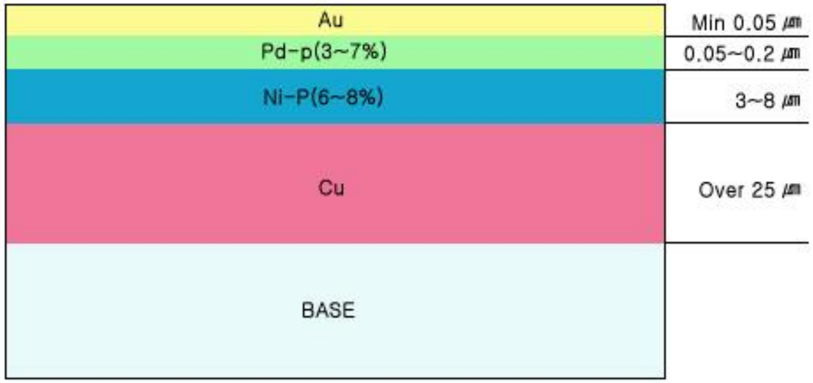
Brittle SnNi intermetallics fail more easily with a high modulus LF solder ball. These cracks resulted from product handling.

ENEPIG

- Electroless nickel, electroless palladium, immersion gold
  - Initially aimed at IC packages and microelectronics
  - Most common lead finish after tin



- Thicknesses
  - Nickel: 5um / 200 µin (120-240)
  - Palladium: 0.15um / 6 µin (2-15)
  - Gold: 0.1um / 4 µin (2 to 8)



ENEPIG Advantages

- Long-term storage (similar to ENIG)

- Solderable and wire bondable (unlike ENIG)
  - Gold and aluminum wire bonds
  - Traditional surface finishes would require ENIG (electroless nickel, immersion gold) over the SMT pads and an additional soft bondable gold over the wire bond pads.
  - Combined cost of ENIG and soft bondable gold process can be more than the higher raw material price of ENEPIG

- NO black pad (unlike ENIG)

ENEPIG Concerns

- Need to maintain control over palladium thickness
  - When used as lead finish, thick palladium can sometimes result in wetting issues
- Does not wet as well as HASL
- Not widely available
- More complex process
  - Three plating steps; violates keep it simple (KIS) principle

ENEPIG Concerns

- Thick palladium can also result in decrease in solder joint strength (grams-force), adverse effect on fracture mode
  - score for fracture mode after the completion of solder ball pull testing

Results of Solderability Testing

	Au um								
Pd um	0.03	0.05	0.07	0.1	0.15	0.2	0.25	0.3	0.4
0.01	90	90	90	90	90	80	80	55	60
0.02	100	100	100	100	100	90	90	90	90
0.03	100	100	100	100	100	100	100	100	90
0.05	100	100	100	100	100	100	100	100	90
0.07	100	100	100	100	100	100	90	90	90
0.10	90	90	90	90	90	90	80	80	80
0.12	85	85	83	8	80	80	60	73	55
0.15	50	60	60	55	55	55	55	60	
0.20	50	60	50	55	58	60	30	35	30
0.30	20	45	40	30	20	30	20	30	30

Uyemura, G. Milad, Study of Suitable Palladium and Gold Thickness in ENEPIG Depositsfor Lead Free Soldering and Gold Wire Bonding

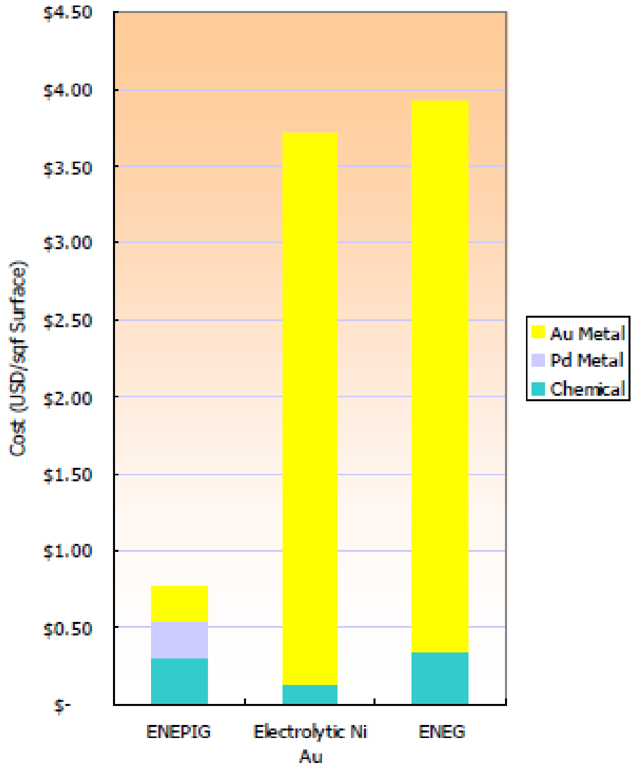
Direct Immersion Gold

- Combination immersion and electroless
  - Claims of pore-free gold surface
  - Normal immersion gold has trouble properly attaching to copper surface
- Developed specifically for parts where nickel could create RF interference.
- To avoid the inherent problems of copper migration through the thin gold surface, it is necessary for these parts to go to final assembly within four months
  - Not widely used

Some Cost Information

ROHM AND HAAS ELECTRONIC MATERIALS
CIRCUIT BOARD TECHNOLOGIES

Cost Comparison



Metal	Oct 06 Average Metal Price (USD/g)	Density (g/cc)		
		Metal	Electrolytic	Electroless
Gold	20.35	19.30	19.00	19.00
Palladium	10.69	12.00	11.90	10.00

Assumptions

- Plating area 15%
- Metal running cost includes processing charge

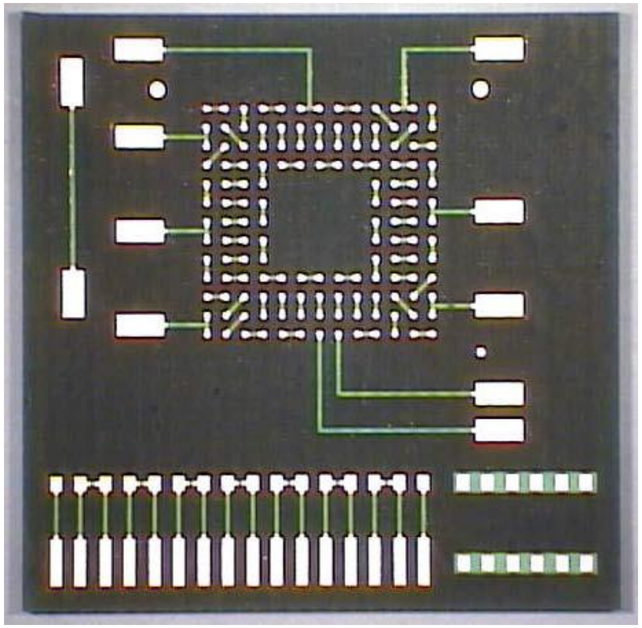
Deposit Thickness (µm)	ENEPIG	E'lytic Ni/Au	ENEG
Gold	0.03	0.5	0.5
Palladium	0.1	-	-

Dennis Yee, April 2007

DfR Solutions

ENEPIG – Raytheon Reliability Study

- ENEPIG Reliability Conclusions
  - Visual, Functional, X-Ray and Shear Tests All Passed
  - Trace Durability Tests Passed
  - Pd Thickness Had No Effect on Wire Bond Results
  - Suppliers, Designs and Applications Outside the Scope of the Work Seek Further Validation
  - ENEPIG Has Potential as a Viable Low Cost Board Finish for Wire Bonding and Sn63 Soldering



  - Details courtesy of Mike Wolverton, P.E. Raytheon Company, 2011

Surface Finish Selection Guideline

Product Attributes

Cost Sensitive Product

High Volume Required

Cosmetics of Finish is Important

High Yield ICT Required

Pb-Free HASL

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

Wire bonding to Finish is Required

Capable

Not Capable

Solderability Plating: Pb-Free HASL

- Increasing Pb-free solderability plating of choice
- Primary material is Ni-modified SnCu (SN100CL)
  - Initial installations of SAC being replaced
- Selection driven by
  - Storage
  - Reliability
  - Solderability
  - Planarity
  - Copper Dissolution

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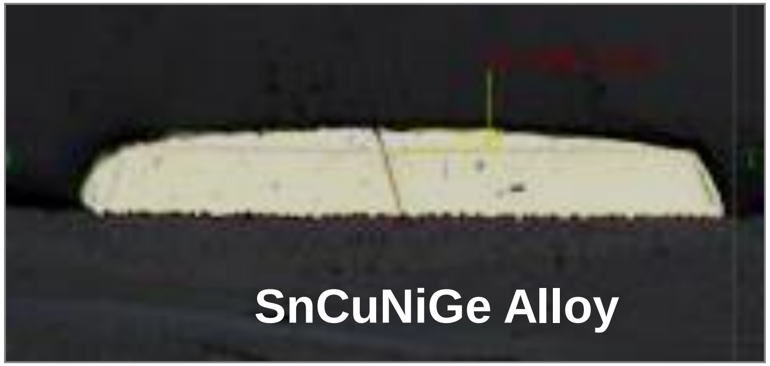
Pb-Free HASL: Ni-modified SnCu

- Alloy selection is critical.
  - Sn-Cu will result in high Cu dissolution and poor planarity.
  - SnCuNiGe provides high fluidity and reduced Cu dissolution.



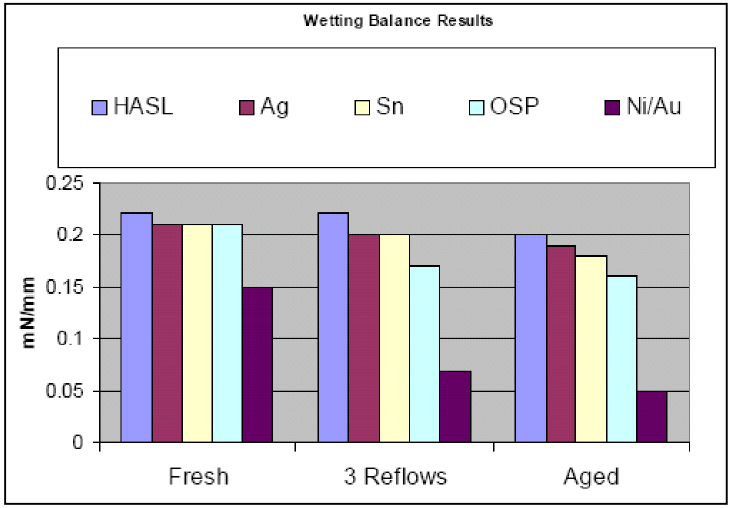
- Role of constituents
  - **Cu** creates a eutectic alloy with lower melt temp (227C vs. 232C), forms intermetallics for strength, and reduces copper dissolution
  - **Ni** suppresses formation of β-Sn dendrites, controls intermetallic growth, grain refiner
  - **Ge** prevents oxide formation (dross inhibitor), grain refiner

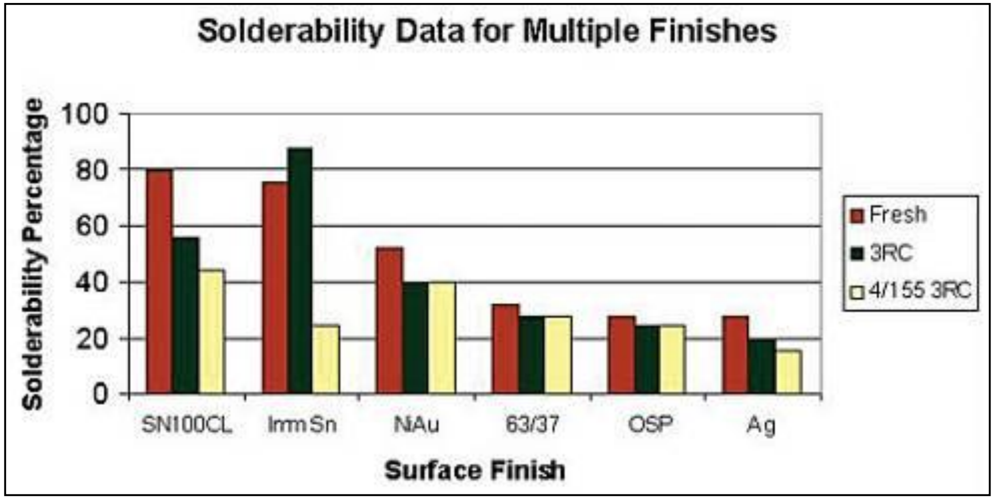
Pb-free HASL: Storage

- PCBs with SnPb HASL have storage times of 1 to 4 years
  - Driven by intermetallic growth and oxide formation
- SN100CL demonstrates similar behavior
  - Intermetallic growth is suppressed through Ni-addition
  - Oxide formation process is dominated by Sn element (similar to SnPb)
- Limited storage times for alternative Pb-free platings (OSP, Immersion Tin, Immersion Silver)

Pb-Free HASL: Solderability

- Industry adage: Nothing solders like solder





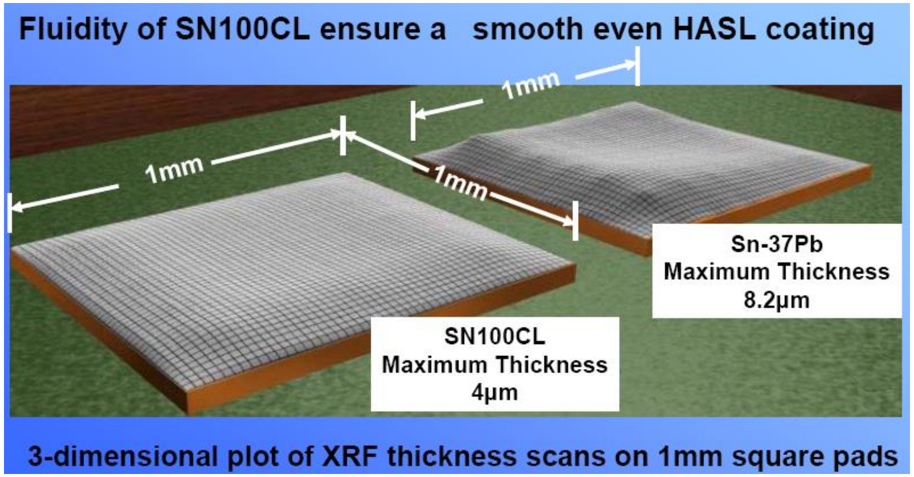
- Discussions with CMs and OEMs seem to indicate satisfaction with Pb-free HASL performance
  - Additional independent, quantitative data should be gathered
- Improved solderability could improve hole fill

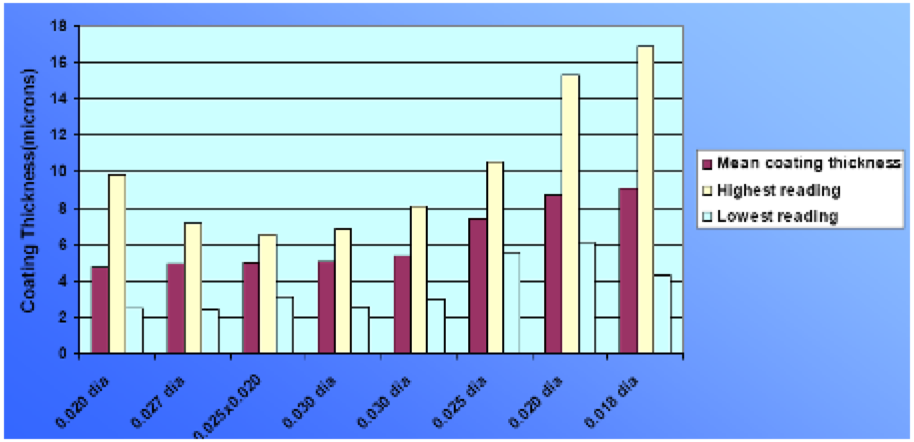
http://www.daleba.co.uk/download%20section%20-%20lead%20free.pdf

HASL and Flow: A Lead-Free Alternative, T. Lentz, et. al., Circuitree, Feb 2008, http://www.circuitree.com/Articles/Feature_Article/BNP_GUID_9-5-2006_A_10000000000000243033

Pb-Free HASL: Planarity

- Recommended minimum thickness
  - 100 uin (4 microns)
  - Lower minimums can result in exposed intermetallic
- Primary issue is thickness variability
  - Greatest variation is among different pad designs
  - 100 uin over small pads (BGA bond pads); over 1000 uin over large pads
- Can be controlled through air knife pressure, pot temperatures, and nickel content





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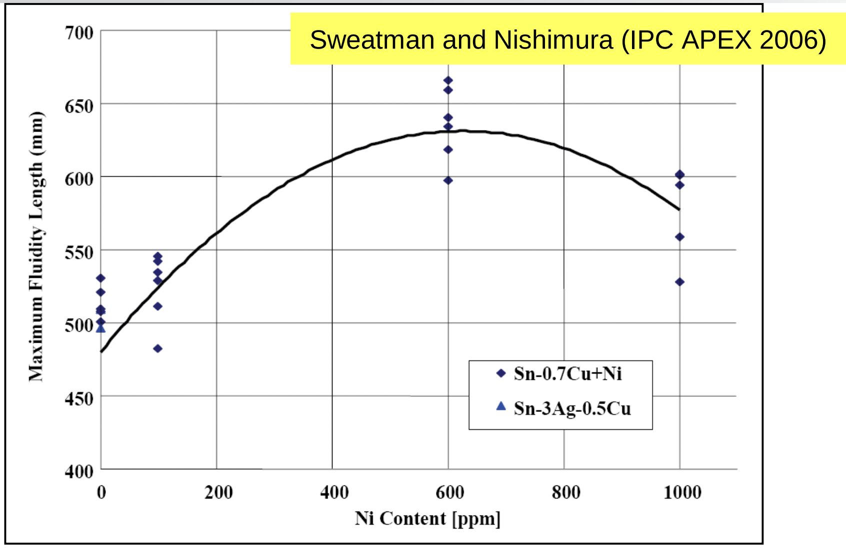
Pb-Free HASL: Planarity (cont.)

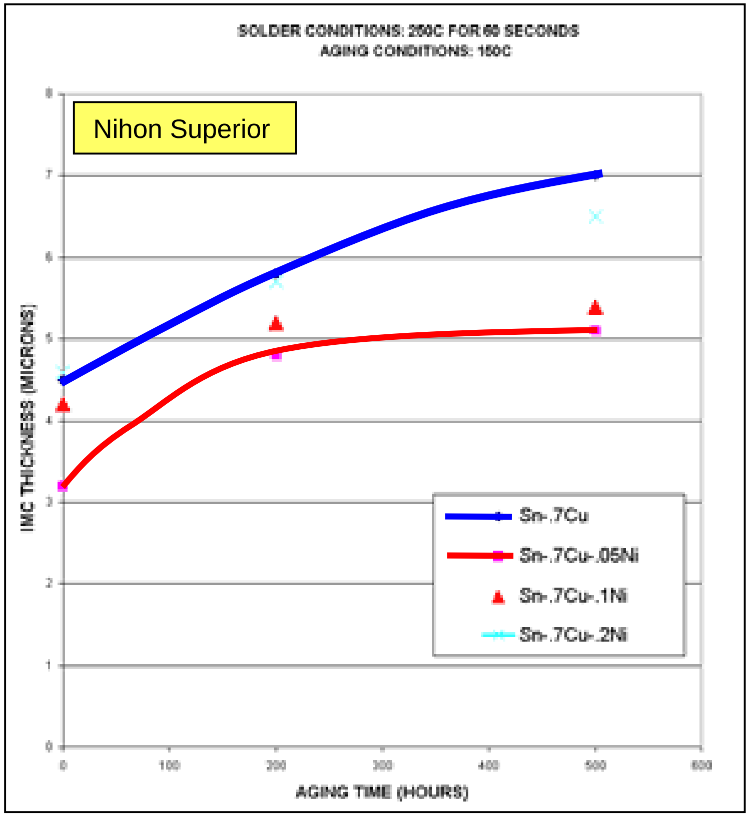
- Air knives
  - Pb-free HASL requires lower air pressure to blow off excess solder
- Pot Temperatures
  - SnPb: 240C to 260C
  - SN100CL: 255C to 270C (air knife temp of 280C)
- Ni content
  - Variation can influence fluidity
    - Minimum levels critical for planarity
  - Some miscommunication as to critical concentrations

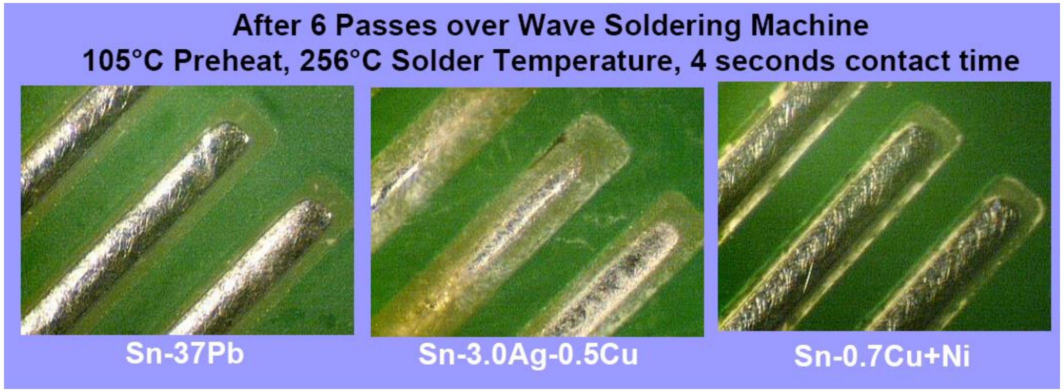


DfR Solutions

Pb-Free HASL: Copper Dissolution

- Presence of nickel is believed to slow the copper dissolution process
  - SAC HASL removes ~5 um
  - SNC HASL removes ~1 um





www.p-m-services.co.uk/rohs2007.htm

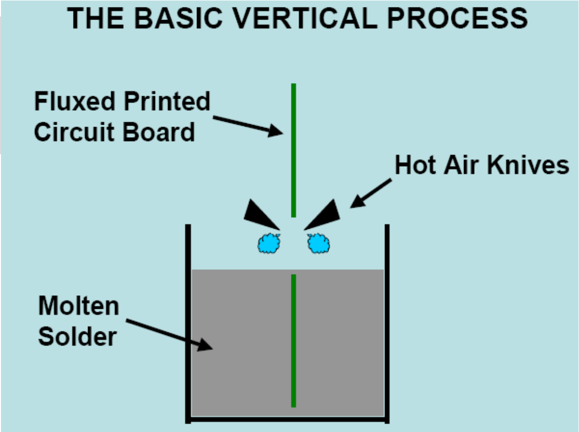
www.pb-free.org/02_G.Sikorcin.pdf

www.evertiq.com/news/read.do?news=3013&cat=8 (Conny Thomasson, Candor Sweden AB)

Pb-Free HASL: Additional Concerns

- Risk of thermal damage, including warpage and influence on long term reliability (PTH fatigue, CAF robustness)
  - No incidents of cracking / delamination / excessive warpage reported to DfR to date
  - Short exposure time (3 to 5 seconds) and minimal temp. differential (+5°C above SnPb) may limit this effect
- Compatibility with thick (>0.135") boards
  - Limited experimental data (these products are not currently Pb-free)
- Mixing of SNC with SAC
  - Initial testing indicates no long-term reliability issues (JGPP, Joint Group on Pollution Prevention)

LF HASL – Critical Parameters



Pre-Clean:

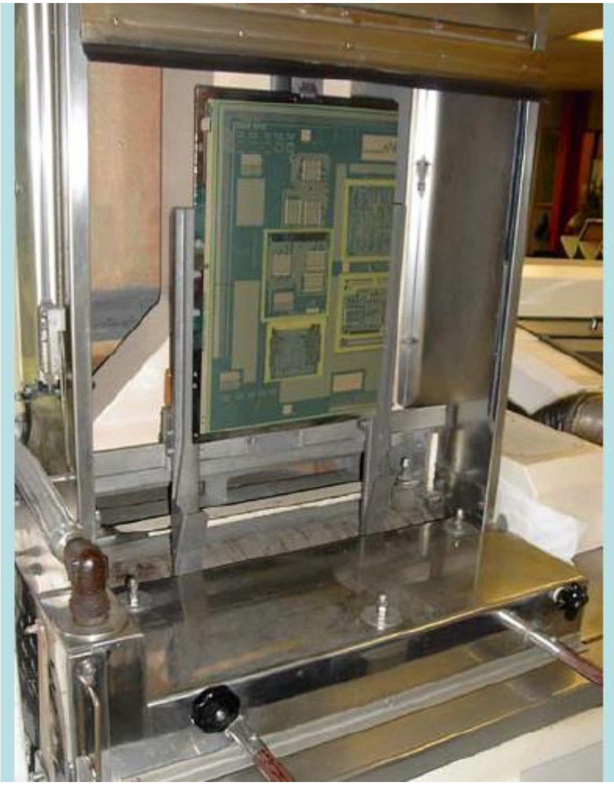
- Micro-etching rate
- Flux

HASL:

- LF Alloy
- Pot temperature (~265C)
- Front & Back air knife pressure
- Front & Back air knife angle
- Distance between air knife & PCB
- Lifting speed
- Dwell time (~ 2-4 sec)

Post-Clean:

- Final flux clean and rinsing



Newer Finishes to the Market

Product Attributes

Cost Sensitive Product

High Volume Required

Lower cost than ENIG

Cosmetics of Finish is Important

High Yield ICT Required

EPd

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

Needs verification

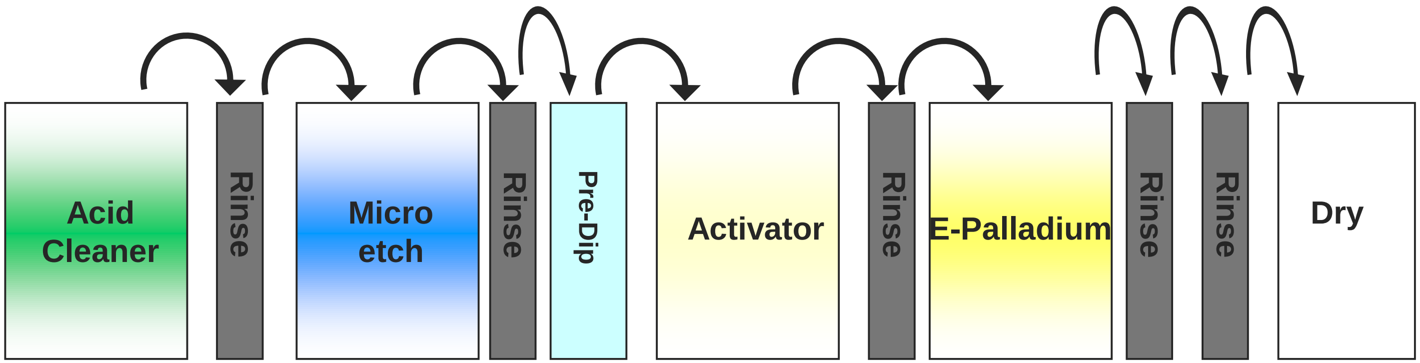
Wire bonding to Finish is Required

Capable

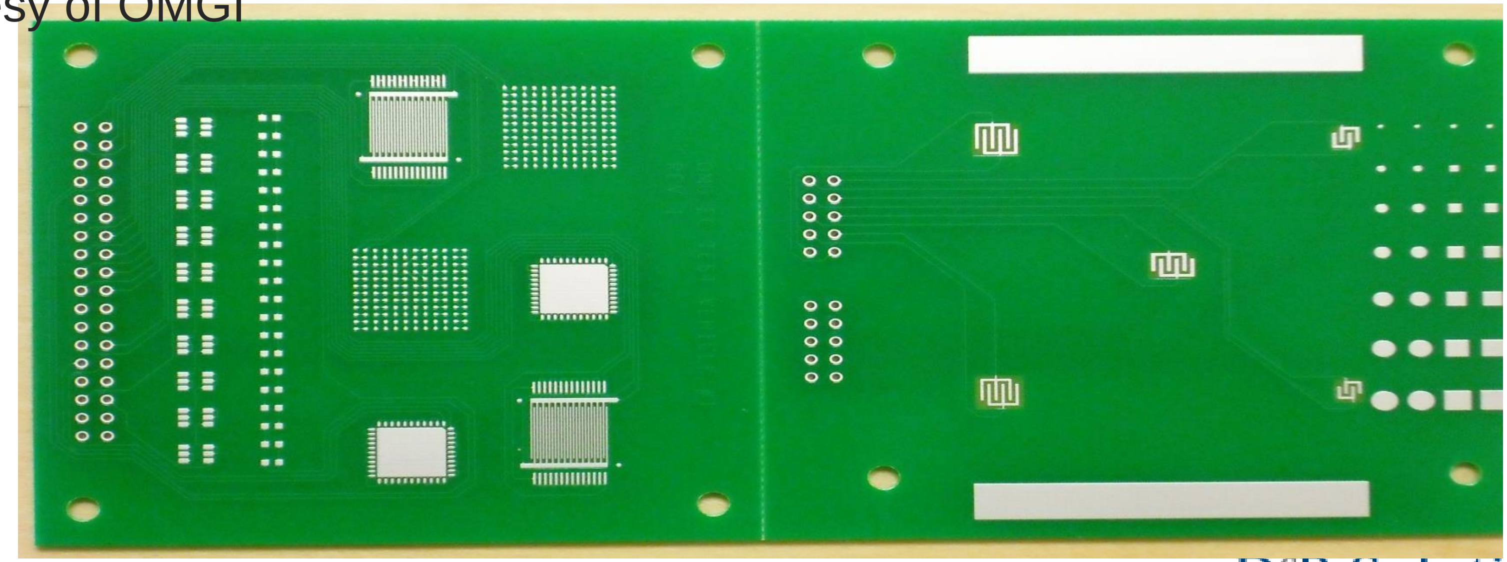
Not Capable

Electroless Pd

Process Sequence



Courtesy of OMGI



DfR Solutions

Newer Finishes to the Market

Product Attributes

Cost Sensitive Product

High Volume Required

These will become more favorable with time.

Cosmetics of Finish is Important

High Yield ICT Required

Nanofinish & Plasma

Pb-Free Wave Solder (PCB > 62mil)

Pb-Free Shock/Drop is a Concern

Fine Pitch Components Used

Corrosion Failure is Possible

Wire bonding to Finish is Required

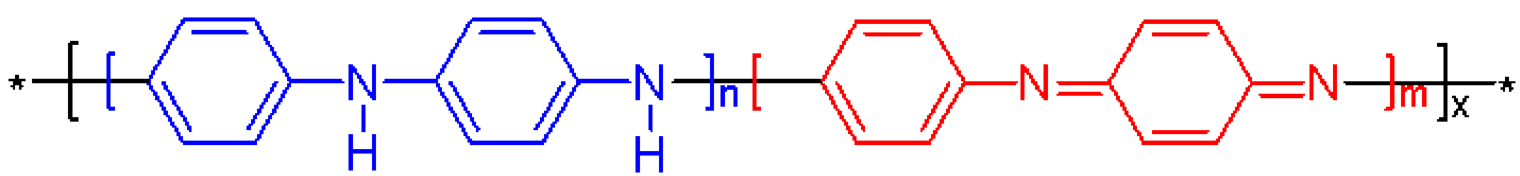
Capable

Not Capable

DfR Solutions

What is Nanofinish?

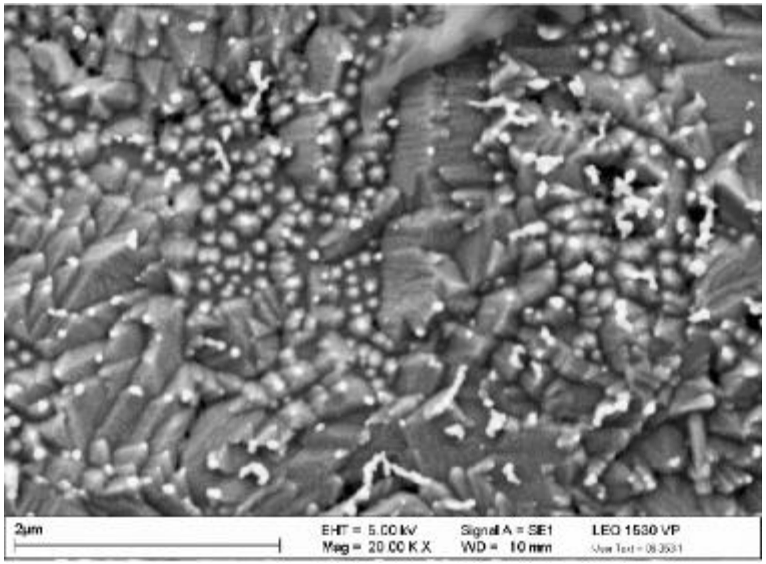
- Nanofinish was released by Ormecon in 2007 (purchased by Enthone in 2008)
  - After 5 to 10 years of research
  - Currently used in structural applications (e.g., iron)
- Nanofinish is described as an organic nanometal
  - Consists of a conductive polymer (polyaniline) complexed with nanoparticles of silver
  - Total thickness is 50 nm; silver particles are nominally 4 nm



Chemical structure of polyaniline (PNI or PANI)

How does Nanofinish work?

- The process of passivation is different from other surface finishes
  - Finish is preferentially deposited on the grain boundaries



- Grain boundaries are high energy area most prone to oxidation
  - Conduction helps passivate copper by lowering the energy levels

DfR Solutions

Why Nanofinish?

- Similar advantages to OSP
  - Bonding is to copper (stronger than bonding to nickel)
  - Few number of process steps
- Some advantages over OSP
  - Conductivity is better for in-circuit testing
  - Supposedly superior performance in regards to number of reflows (>10) and long-term aging

ACL 7002 Cleaner (2 min)
MET 7002 Etch (2 min)
DI-Rinse
CND 7200 Predip (60 s)
OMN 7200 Nanofinish (90 s)
DI-Rinse Drying

Market for Nanofinish

- Lots of interest; still limited penetration
- Largest users or most receptive were in Asia (Korea, China) and some in Germany
- Market strategy was directed at OEMs

Assessment of Nanofinish

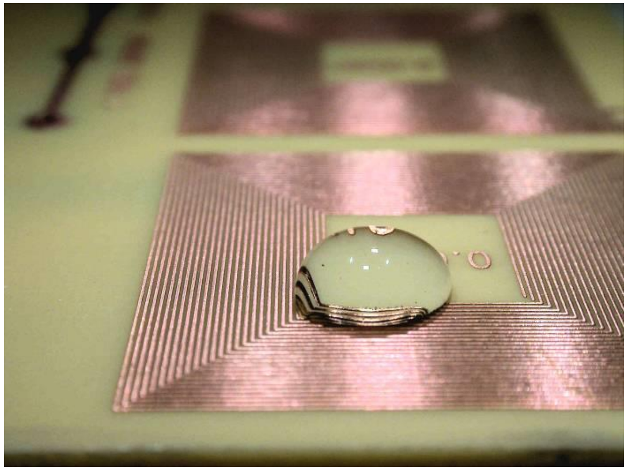
- Must consider material set
  - Conductive polymers are known to be sensitive to moisture
  - Silver is known to be reactive with sulfur

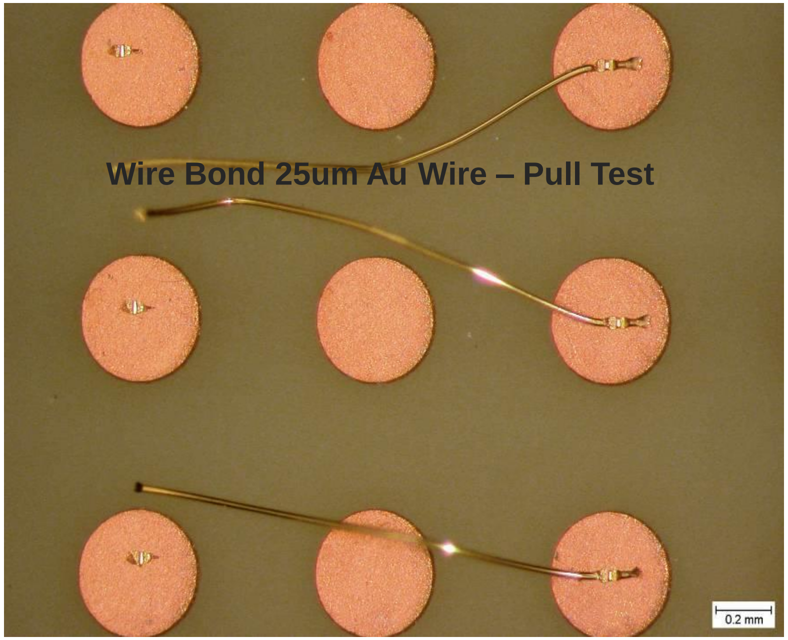
- Test coupon must be similar to board design
  - Through holes
  - Solder mask
  - Similar feature sizes

- Testing should go beyond steam aging and mixed flowing gas (MFG)

Plasma Coated Finish

- Coated in plasma chamber.
- Many panels coated simultaneously.
- Film is 60 nm thick.
- Flux breaks through film at elevated temperature.
- Hydrophobic and acid resistant





Courtesy of Semblant

Semblant

- Utilizes plasma polymerization to deposit an ultrathin protective coating on the surface of a PCB
  - Extremely hydrophobic
- Extended PCB shelf life
  - Long term protection against oxidation
  - Corrosion resistance

- Acceptable solderability
  - Compatible with SnPb and Pb-free reflow processes

Semblant Plasma Finish

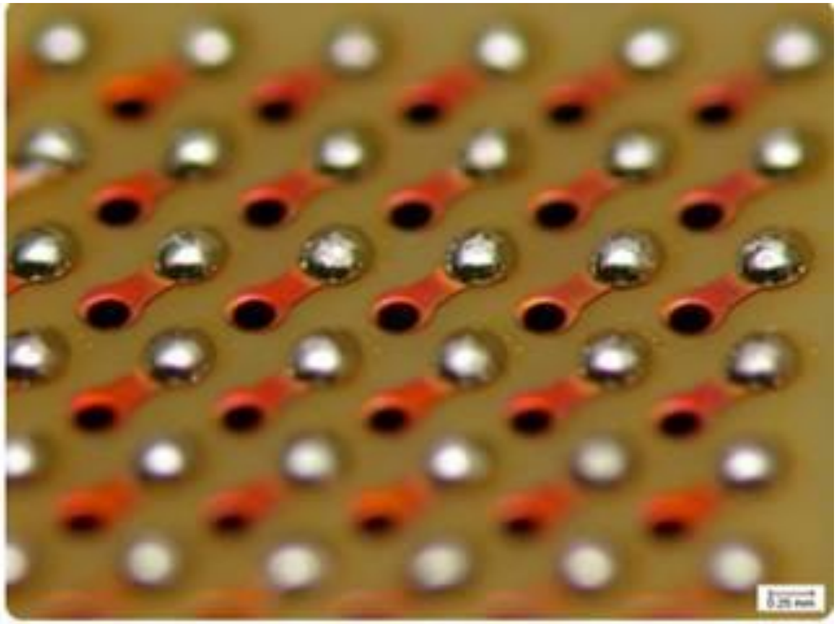
- Uses a fluoropolymer coating in a room temperature process.
  - The plasma deposition is combined with a pre-cleaning step
- Creates a continuous film that is 10's of nanometers thick everywhere the active gas plasma comes into contact with the surface – including through vias.
- The SPF fluoropolymer has stable chemical properties
  - Resistant to heat (up to 40 minutes at 260C)
  - Resistant to chemicals (non-reactive to flux at room temp)

Semblant Finish (cont.)

- The Semblant fluoropolymer is removed by the combined action of the acidic flux and the high temperatures used during reflow, resulting in a direct Cu/Sn solder joint.
  - The unoxidized copper beneath the SPF coating ensures wettability of the solder.
  - The surrounding fluoropolymer film prevents the solder from spreading beyond the printed area, reducing bridging and enabling ultra-fine pitch assembly.

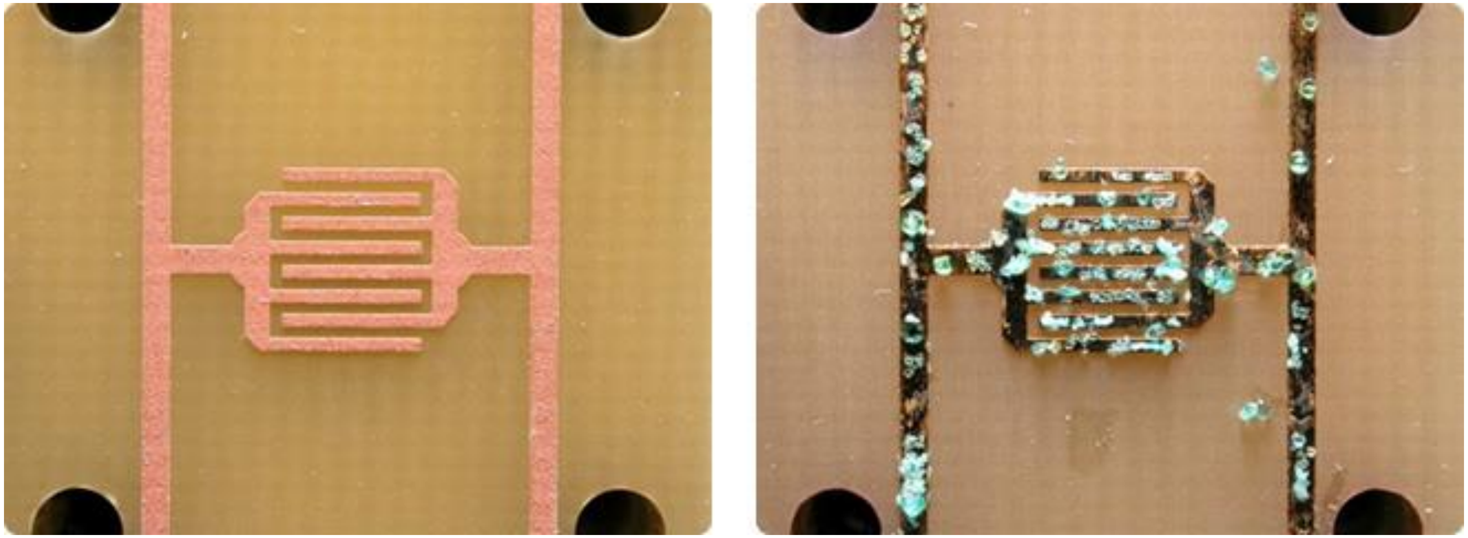
Plasma Finish - Advantages

- Solder mask and solderability plating in one



Advantages (cont.)

- Protection against corrosive gases
    - Actively repelling water and preventing corrosive gasses from coming into contact with the copper surface.



Plasma coating vs. ENIG (elevated sulfur gas testing

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Challenges

- Will require redesign of stencils and optimization of some manufacturing processes
  - No flux? No wetting
  - Can not rely on solder alone

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Examples of Best Application Fits

- OSP (but must address ICT issues)
  - Hand held electronics
  - Notebook computers
  - Basic desktop computers
  - Basic consumer electronics & power supplies
  - Simple Pb-free Medical or aerospace (thin PCBs)
- ENIG or ENEPIG
  - SnPb medical and aerospace
  - Pb-free that is not susceptible to shock

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Examples of Best Fits

- ImAg
  - Fully enclosed hand held electronics
  - Basic consumer electronics – low power and airflow
- ImSn
  - Simple consumer electronics (not fully enclosed)
  - Simple medical or aerospace applications (1 side)
  - Low to moderate volume peripheral components
- LF HASL
  - Thick LF PCBs going into business environments (servers, telecom equipment)
  - Complex Pb-Free medical or aerospace?

What to do if there is no SF fit?

- If no SF fits your specific requirements, design modifications may be required and tradeoffs made
- For example, I need low cost, high volume, corrosion resistant, with good ICT capability
  - One solution might be to use ImAg but plug the vias with soldermask to protect from corrosion (but some cost is sacrificed)
  - Another is to use OSP but implement cleaning to remove flux residue for probing (cost is again sacrificed)

Example #2

- Another example might be the desire to use ENIG for a Pb-free product where shock is a concern.
  - One solution might be to underfill critical components sensitive to shock (cost adder).
  - Another might be to dampen the shock by better design of the enclosure (possible cost adder).

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Summary

- Surface finish selected has a large influence on quality, reliability and cost
- Complex decision that impacts many areas of the business
- Select a finish that optimal for the business (and not just one function)
- Know that there are engineering tricks to improve on weak areas of each finish
- Stay current in this field because new developments continue to be made

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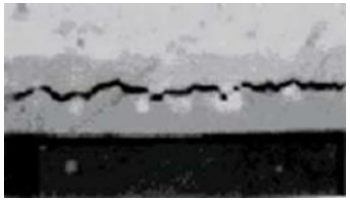
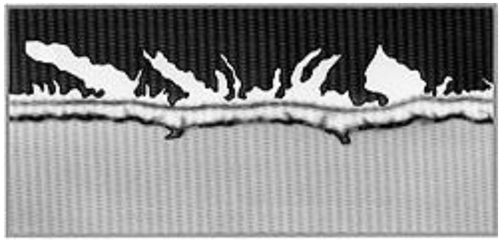
PCB Storage

Printed Circuit Board Storage

- If you have always used SnPb HASL plated boards, the biggest change will be storage times
- Except for ENIG, which many companies avoid because of cost, all alternative Pb-free platings should be limited to 12 months of storage
- Over time ImSn will form intermetallics (temperature), OSP-coated copper will oxidize (humidity), and ImAg will tarnish (gaseous sulfides)





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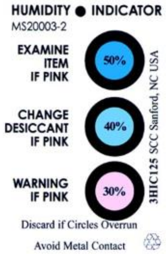
Shipping & Handling

- PCBs should remain in sealed packaging until assembly
- Package PCBs in brick counts which closely emulate run quantities
- PCBs should be stored in temperature and humidity controlled conditions
- Packaging in MBB (moisture barrier bags) with desiccant and HIC (humidity indicator cards) may be needed for some laminates

Vacuum Sealer



Humidity Indicator Card

Moisture Barrier Bag

Best Practices for Improving the PCB Supply Chain

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PCBs as Critical Components

- PCBs should always be considered critical components
  - Custom design
  - Product Foundation
- Long term PCB quality and reliability is simply not achievable without stringent controls in place for:
  - Supplier selection
  - Qualification
  - Management

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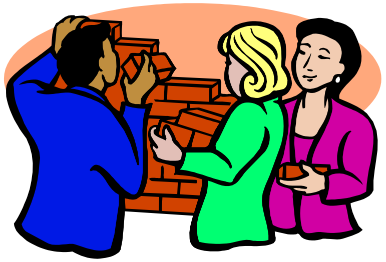
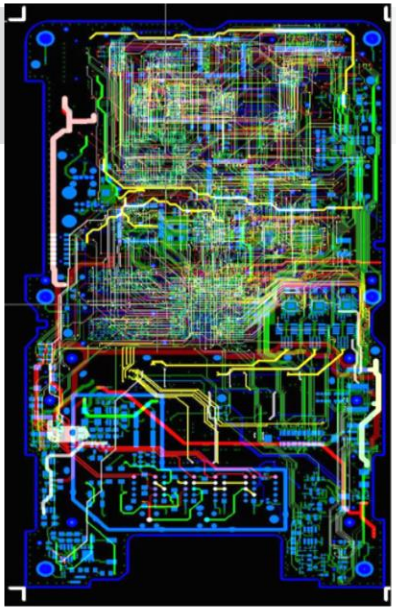
PCB Procurement Team

- Create a PCB Procurement Team with at least one representative from each of the following areas:
  - Design
  - Manufacturing
  - Purchasing
  - Quality/Reliability



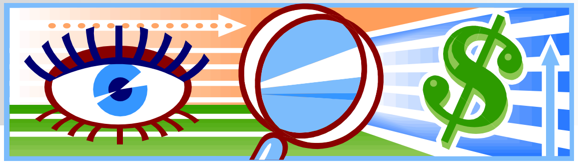
- Team should meet on a routine basis
  - Discuss new products and technology requirements in the development pipeline.
  - Pricing, delivery, and quality performance issues with approved PCB suppliers should also be reviewed.
- Team is also tasked with identifying new suppliers and creating supplier selection and monitoring criteria

Supplier Selection Criteria



- Established PCB supplier selection criteria in place.
  - Criteria should be custom to your business
- Commonly used criteria are:
  - Time in business
  - Revenue
  - Growth
  - Employee Turnover
  - Training Program
  - Certified to the standards you require (IPC, MIL-SPEC, ISO, etc.)
  - Capable of producing the technology you need as part of their mainstream capabilities
  - Don’t exist in PCB process “niches” where suppliers claim capability but have less than ~ 15% of their volume built there
  - Have quality and problem solving methodologies in place
  - Have a technology roadmap
  - Have a continuous improvement program in place

PCB Qualification Criteria



- Rigorous qualification criteria which includes:
  - On site visit by to the facility which will produce your PCBs by someone knowledgeable in PCB fabrication techniques.
    - Review process controls, quality monitoring and analytical techniques, storage and handling practices and conformance to generally acceptable manufacturing practices.
    - Best way to meet and establish relationships with the people responsible for manufacturing your product.
  - Sample builds of an actual part you will produce which are evaluated by the PCB supplier
    - Also independently evaluated by you or a representative to the standards that you require.

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PCB Supplier Tiering

- Use of supplier tiering
  - Low, Middle, High strategies if you have a diverse product line with products that range from simpler to complex
    - Allows for strategic tailoring to save cost and to maximize supplier quality to your product design
    - Match supplier qualifications to the complexity of your product. Typical criteria for tiering suppliers include:
  - Finest line width
  - Finest conductor spacing,
  - Smallest drilled hole and via size
  - Impedance control requirement
  - Specialty laminate needed (Rogers, flex, mixed)
  - Use of HDI, micro vias, blind or buried vias.
- Minimize use of suppliers who have to outsource critical areas of construction
- Again, do not exist in the margins of process capabilities!

PCB Relationship Management

- Partner with your PCB suppliers for success.
  - Critical for low volumes, low spend, or high technology and reliability requirements
- Some good practices include:
  - Monthly calls with PCB procurement team and each PCB supplier
    - PCB supplier team should members equivalent to your team members
  - QBRs (quarterly business reviews)
    - Review spend, quality, and performance metrics, and "state of the business ", business growth, new product and quoting opportunities…
    - Address any upcoming changes
      - Factory expansion, move, or relocation, critical staffing changes, new equipment/capability installation etc.
    - Twice per year, QBRs should be joint onsite meetings which alternate between your site and the supplier factory site.
      - Factory supplier site QBR visit can double as the annual on site visit and audit that you perform.

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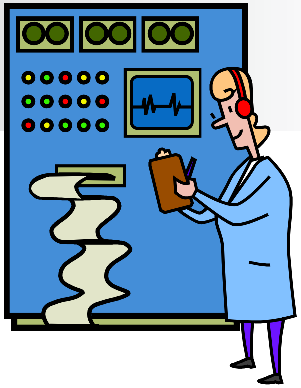
PCB Supplier Scorecards

- Use Supplier Scorecards
  - Perform quarterly and yearly on a rolling basis
- Typical metrics include:
  - On Time Delivery
  - PPM Defect Rates
  - Communication – speed, accuracy, channels, responsiveness to quotes
  - Quality Excursions / Root Cause Corrective Action Process Resolution
  - Supplier Corrective Action Requests
  - Discuss recalls, notifications, or scrap events exceeding a certain dollar amount

PCB Continuous Quality Monitoring



- Review the following:
  - Top 3 PCB factory defects:
    - Improvement, monitoring and reporting
  - Product Yield and scrap reports
  - Feedback on issues facing the industry
  - Reliability testing performed (HATS, IST, solder float, etc.)
  - Review IPC-9151B, Printed Board Process Capability, Quality, and Relative Reliability (PCQR2) Benchmark Test Standard and Database at:
    - http://www.ipc.org/html/IPC-9151B.pdf
    - PCB suppliers may be part of this activity already

PCB Prototype Development

- Ideally, all PCBs should come from the same factory from start to finish
  - Prototype (feasibility), pre-release production (testability & reliability), to released production (manufacturability)
- Any factory move introduces an element of risk
  - Product must go through setup and optimization specific to each factory and equipment contained there
- While not always possible, all PCBs intended for quality and reliability testing should come from the actual PCB production facility

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Part II: Performing The PCB Process Audit

Everything looks great on paper or on the web……

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Why Perform an Onsite Audit?

- No industry standard methodology for qualifying PCB suppliers
  - Standards do exist for lot-based PCB testing and acceptance within the IPC 6010 series
  - Sourcing follows the "as agreed upon between user and supplier" (AABUS) approach
  - IPC began discussing this gap in 2008 with a Blue Ribbon Committee
    - IPC has recently launched a Validation Business Unit with plans to eventually move towards an IPC Qualified Manufacturers List (QML) for suppliers, including PCBs [3]
  - In the meantime, however, onsite audits remain the best approach

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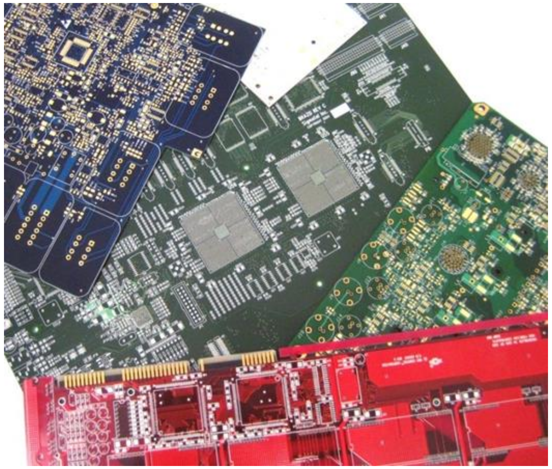
PCB Fabrication Processes

- Knowledge is key!
- Processes are complex, chemistry intensive and there are a lot of steps



More than

180

individual steps required to manufacture typical printed circuit boards

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Audit Focus

- All steps are obviously important but this section will highlight:
  - Requirements
  - Process Control & Analysis
  - Recognizing Common Defects
  - Test & Final Inspection

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Communicate Requirements

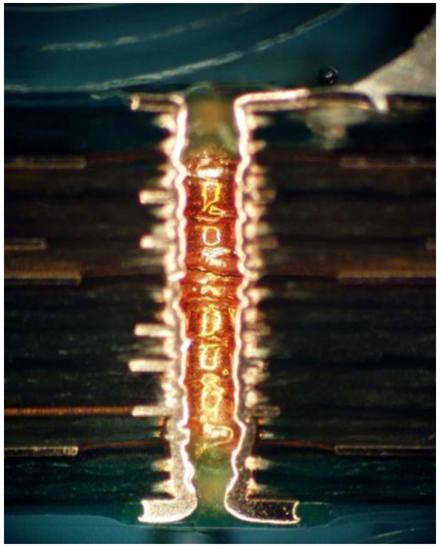
- Define the standards needed
- Communicate both quality & reliability objectives!
  - Help your supplier help you
- Create a PCB Fabrication specification
  - Outlines requirements and communication required for modifications to drawings

Process Control & Analysis

- Cross Sections
  - In process & taken to verify things like:
    - Hole wall quality
    - Desmear / Etchback
    - Plating thickness
    - Dielectric
    - Cross sections of *finished product* are supplied per customer specification.
- Inspections
  - Visual Inspections
  - Automatic Optical Inspection (AOI)
    - Programmed from the gerber data to inspect the etched copper panels.
  - X-Ray Inspection
    - Drilling Performance
    - Layer alignment
  - Cleanliness Measurements

Common PCB Defects

- Basic understanding of common PCB defects is helpful
  - Ask for cross-section images
    - Required for process control
  - Knowledge can be used by an organization to monitor supplier performance over time
  - Insufficient Plating, Voids, Nodules, Folds, Etch Pits, Fiber Protrusion



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Test & Final Inspection

- Electrical Test
  - IPC-D-356 netlist is uploaded into the tester
  - Each PCB is manually placed on fixture and tested for continuity and resistance
    - Verify handling for segregating passes & fails
- Final Inspection
  - Visually inspect 100% of the finished product
  - Review of:
    - Fabrication drawing requirements
    - Dimensional properties
    - Board size
    - Finished hole sizes
    - Customer specification

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PCB Supply Chain Summary

- Foundation of a reliable product is a reliable PCB
  - PCBs are always custom, critical components
- Have a comprehensive strategy for selecting and qualifying PCB suppliers
  - Ensures that the foundation is strong
- Performing effective on site audits is a critical component of that strategy

DfX Summary

- To avoid design mistakes, be aware that functionality is just the beginning. Design reliability in!
- Be aware of industry best practices
- Maximize knowledge of your design as early in the product development process as possible
- Practice design for excellence (DfX)
  - Design for manufacturability
  - Design for sourcing
  - Design for reliability
  - Design for environment

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Conclusions

- Design for Excellence is a valuable process for lowering cost, reducing time-to-market, and improving customer satisfaction
- PoF is a powerful tool that can leverage the value of DfX activities
- Successful DfX / implementation requires the right combination of personnel and tools and time limitations

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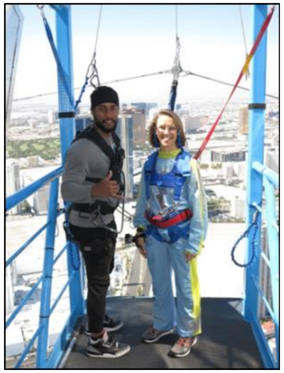
Some Acronyms Defined

- AQL: Acceptable Quality Limit
- AABUS: As Agreed Upon Between User and Supplier
- AVL: Approved Vendor List
- BOM: Bill of Materials
- CAD: Computer Aided Design
- CAM: Computer Aided Manufacturing
- CTE: Coefficient of Thermal Expansion
- DfX: Design for Excellence
- E: Modulus
- FEA: Finite Element Analysis
- ICT: In Circuit Test
- JTAG: Joint Test Action Group
- IPA: Isopropyl Alcohol
- NaCl: Sodium Chloride

- OEM: Original Equipment Manufacturer
- PCB: Printed Circuit Boards
- PLM: Product Lifecycle Management
- PoF: Physics of Failure
- PTH: Plated Through Hole
- PTV: Plated Through Via
- RH: Relative Humidity
- RMA: Rosin Mildly Activated
- SF: Surface Finish
- SIR: Surface Insulation Resistance
- SMT: Surface Mount Technology
- Tg: Glass Transition Temperature
- WOA: Weak Organic Acids

Biography of Content Creator – Cheryl Tulkoff

- Cheryl has over 20 years of experience in electronics manufacturing focusing on failure analysis and reliability. She is passionate about applying her unique background to enable her clients to maximize and accelerate product design and development while saving time, managing resources, and improving customer satisfaction.



- Throughout her career, Cheryl has had extensive training experience and is a published author and a senior member of both ASQ and IEEE. She views teaching as a two-way process that enables her to impart her knowledge on to others as well as reinforce her own understanding and ability to explain complex concepts through student interaction. A passionate advocate of continued learning, Cheryl has taught electronics workshops that introduced her to numerous fascinating companies, people, and cultures.

- Cheryl has served as chairman of the IEEE Central Texas Women in Engineering and IEEE Accelerated Stress Testing and Reliability sections and is an ASQ Certified Reliability Engineer, an SMTA Speaker of Distinction and serves on ASQ, IPC and iNEMI committees.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech and is currently a student in the UT Austin Masters of Science in Technology Commercialization (MSTC) program. She was drawn to the MSTC program as an avenue that will allow her to acquire relevant and current business skills which, combined with her technical background, will serve as a springboard enabling her clients to succeed in introducing reliable, blockbuster products tailored to the best market segment.

- In her free time, Cheryl loves to run! She’s had the good fortune to run everything from 5k’s to 100 milers including the Boston Marathon, the Tahoe Triple (three marathons in 3 days) and the nonstop Rocky Raccoon 100 miler. She also enjoys travel and has visited 46 US states and over 20 countries around the world. Cheryl combines these two passions in what she calls “running tourism” which lets her quickly get her bearings and see the sights in new places.

Thank you!

Cheryl Tulkoff

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