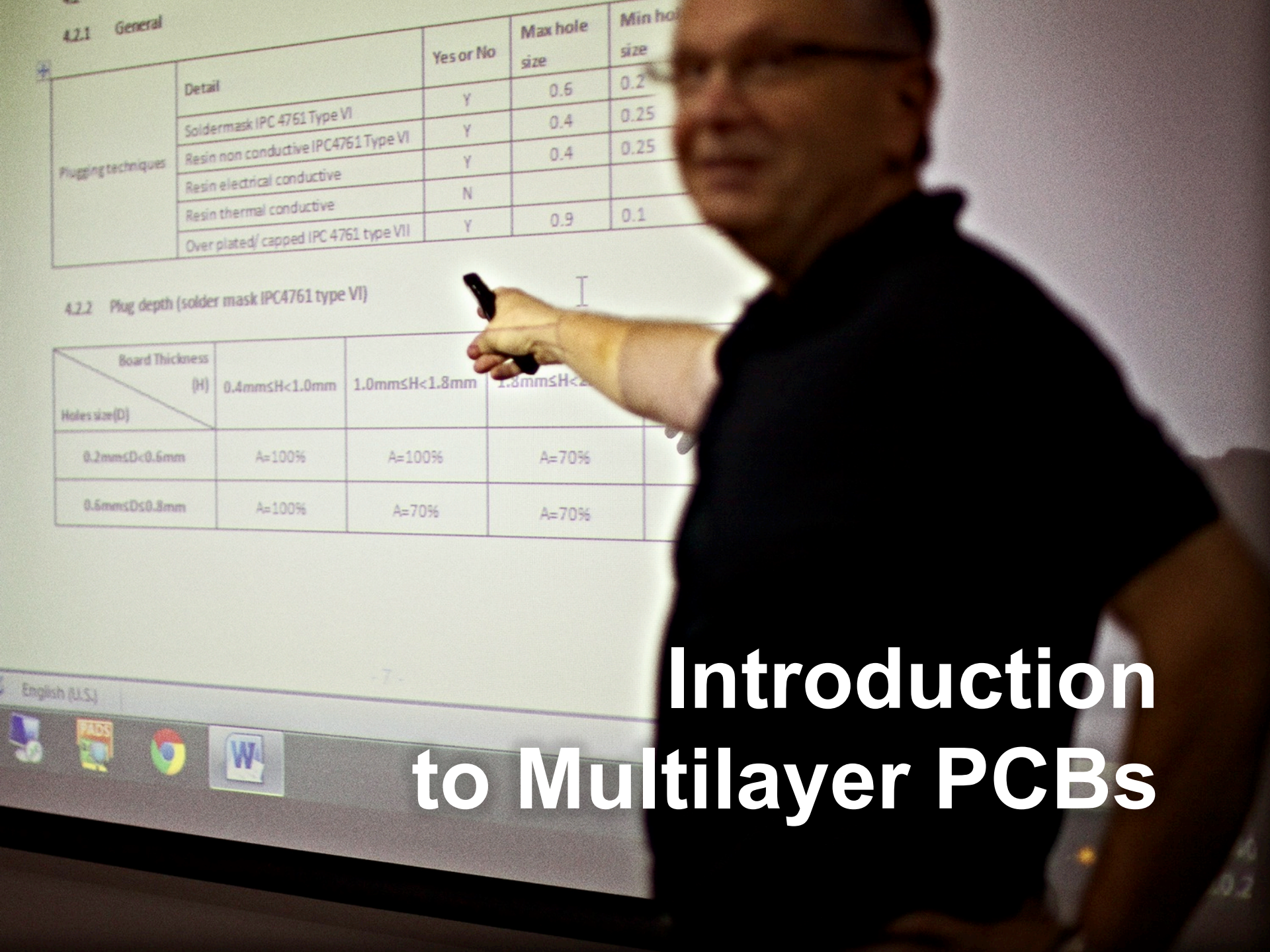
NCAB Group | Seminars

PCB Production Process

– HOW TO PRODUCE A PRINTED CIRCUIT BOARD

NCAB GROUP


4.2.1 General
Detail
Yes or No
Max hole size
Plugging techniques
Soldermask IPC 4761 Type VI
Y
0.6
Resin non conductive IPC4761 Type VI
Y
0.4
0.25
Resin electrical conductive
Y
0.4
0.25
Resin thermal conductive
N
Over plated/ capped IPC 4761 type VII
Y
0.9
0.1
4.2.2 Plug depth (solder mask IPC4761 type VI)
Board Thickness (H)
Holes size(D)
0.4mm≤H<1.0mm
1.0mm≤H<1.8mm
0.2mm≤D<0.6mm
A=100%
A=100%
A=70%
0.6mm≤D≤0.8mm
A=100%
A=70%
A=70%
English (U.S.)
Introduction to Multilayer PCBs

What is a multilayer PCB?

- The green thing with holes in it.
- The **first item needed** when building any electronic product, but often ordered last.
- A **platform** for components.
- Circuitry with pre-defined electrical function.
- Three or more conductive layers of copper which have been bonded to non-conductive substrates, yet are electrically connected where needed, so that they connect specific components using features (tracks and component pads) that have been imaged and etched to form a **bespoke design**, in order to fulfill a **bespoke function**.

History of PCBs

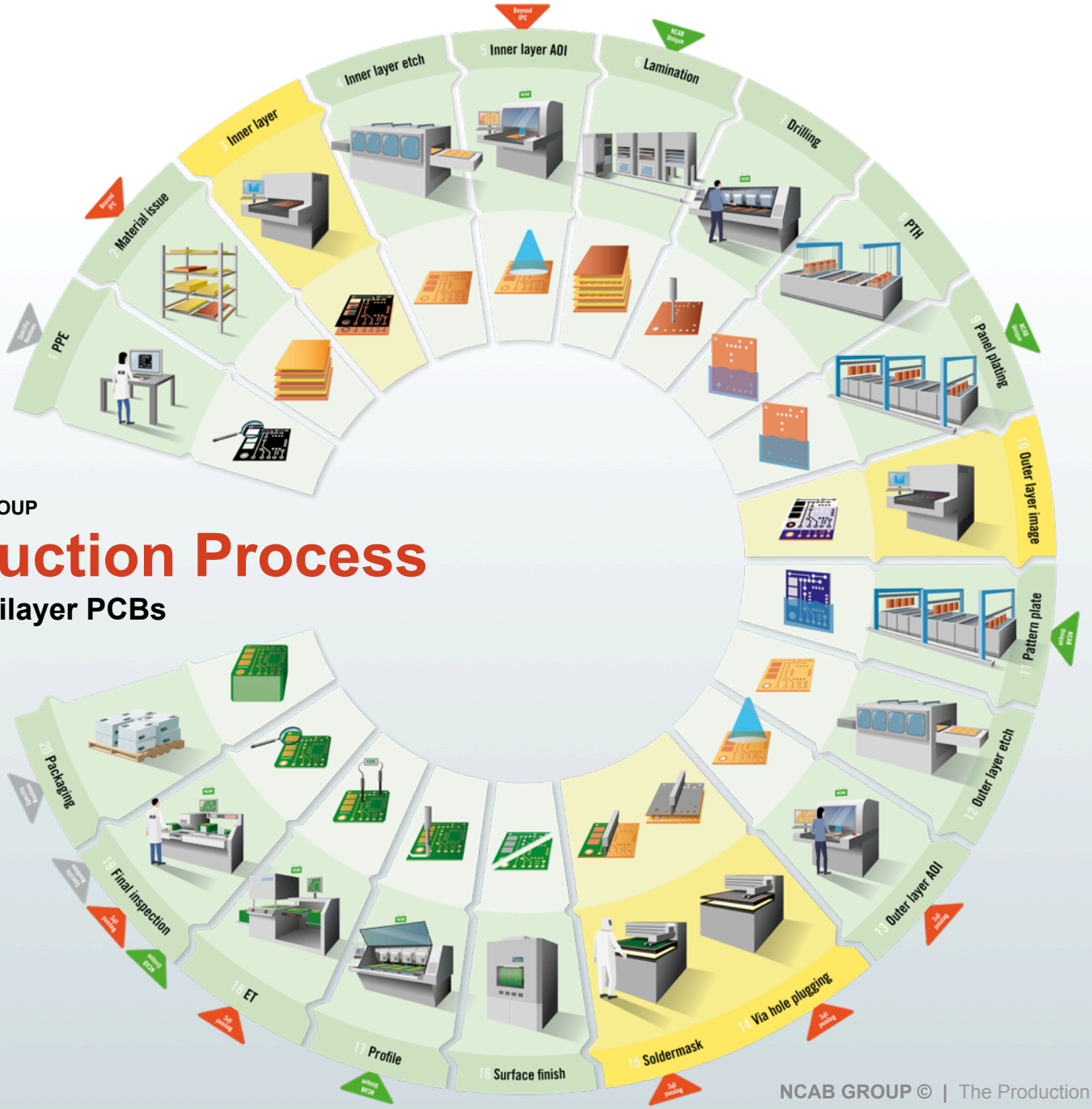
1903	First PCB-patent
1903-1946	Single / double sided boards (NPTH)
1947	Double sided, plated through holes developed
1960	Multilayer process developed.
1993	NCAB was founded
1995	Micro via production
2000	Embedded components


The Production
Process

THE NCAB GROUP

Production Process

– for multilayer PCBs



MANUFACTURING PROCESS

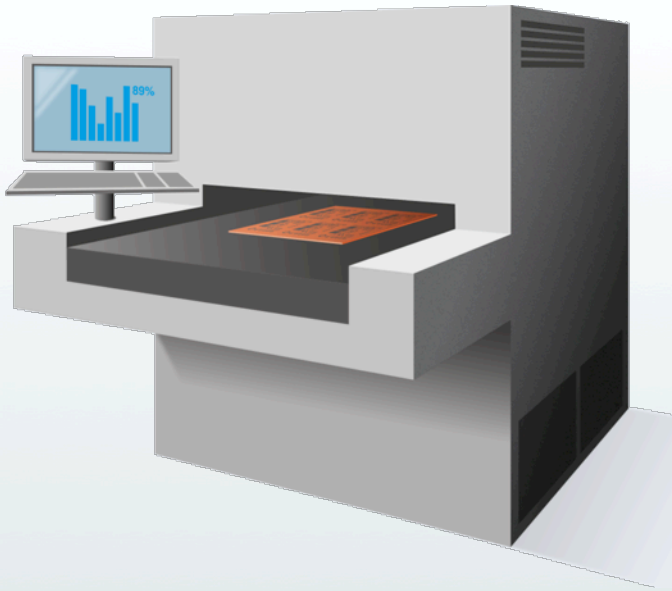
#2 – Material issue

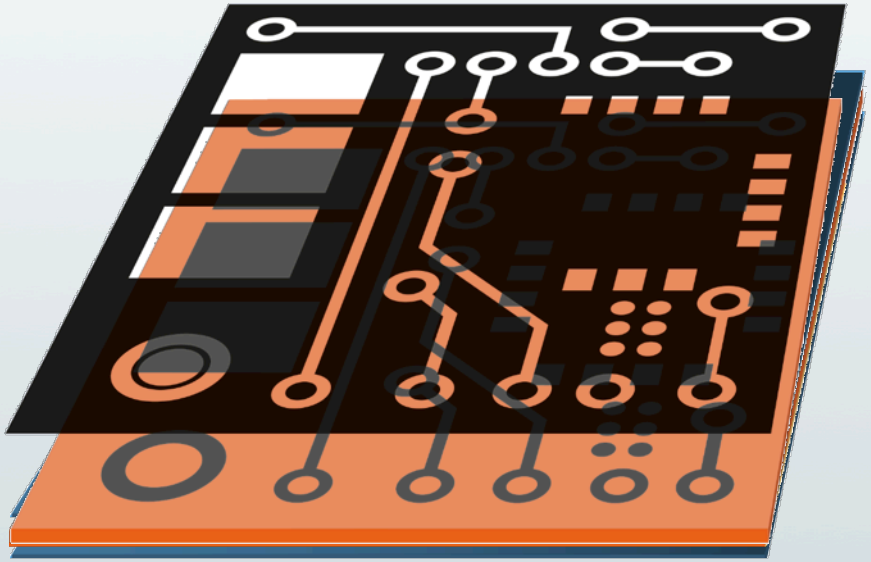
Base material is cut from sheets / larger sizes to working panel sizes.

MANUFACTURING PROCESS

#3 – Inner layer

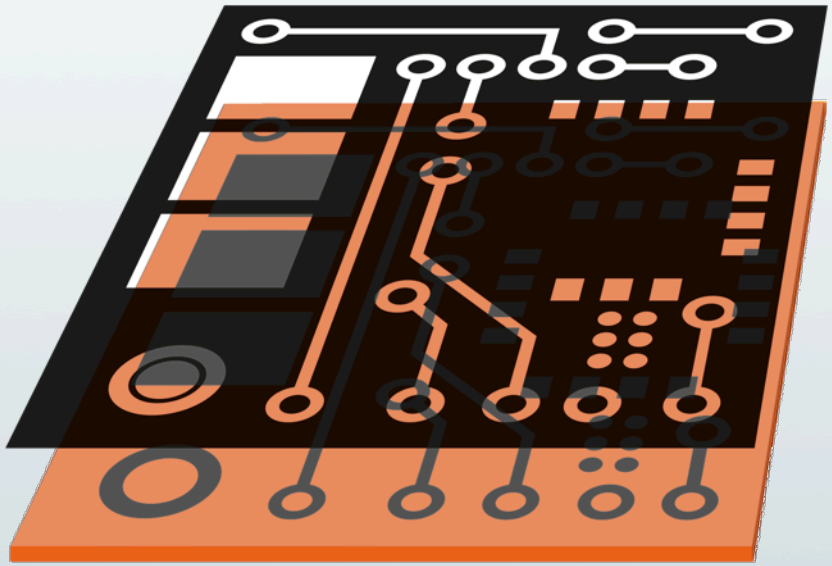
Transfer the image from the artwork to the board surface using photosensitive dry-film and exposure to UV light.





MANUFACTURING PROCESS

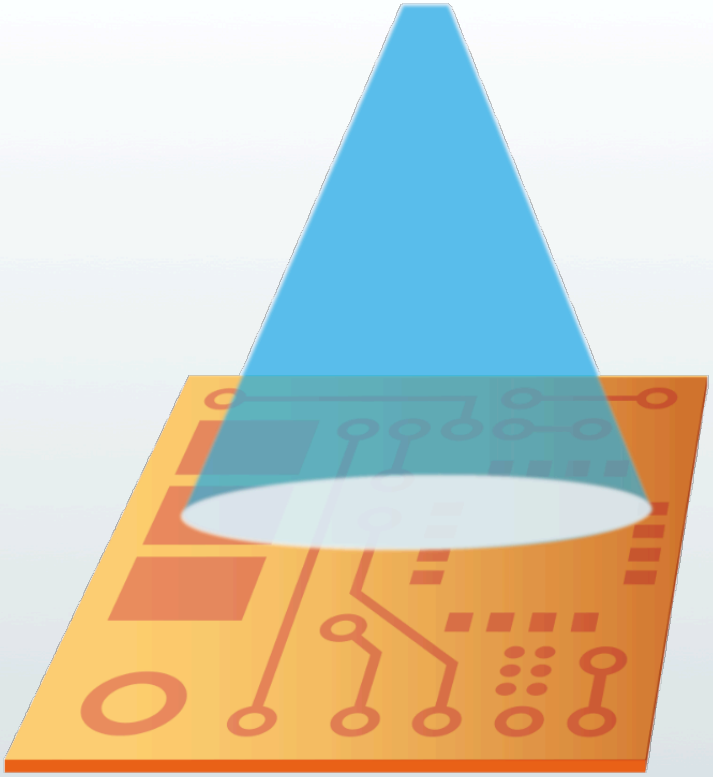
#4 – Inner layer etch



Removal of the unwanted copper (**not** protected by film) from the panel through etching, to leave copper circuitry that matches the image.

MANUFACTURING PROCESS

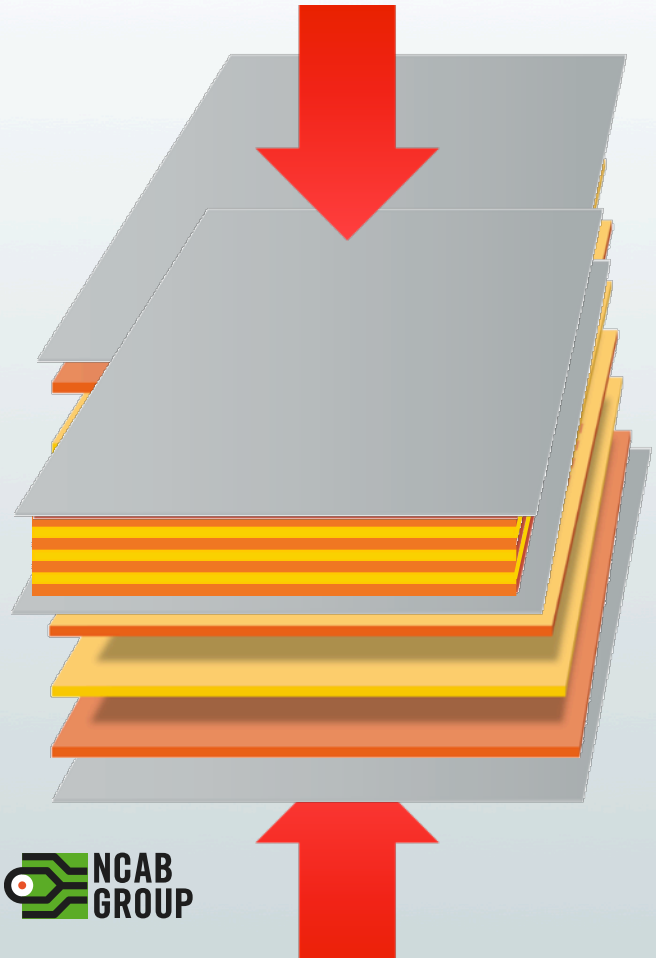
#5 – Inner layer AOI

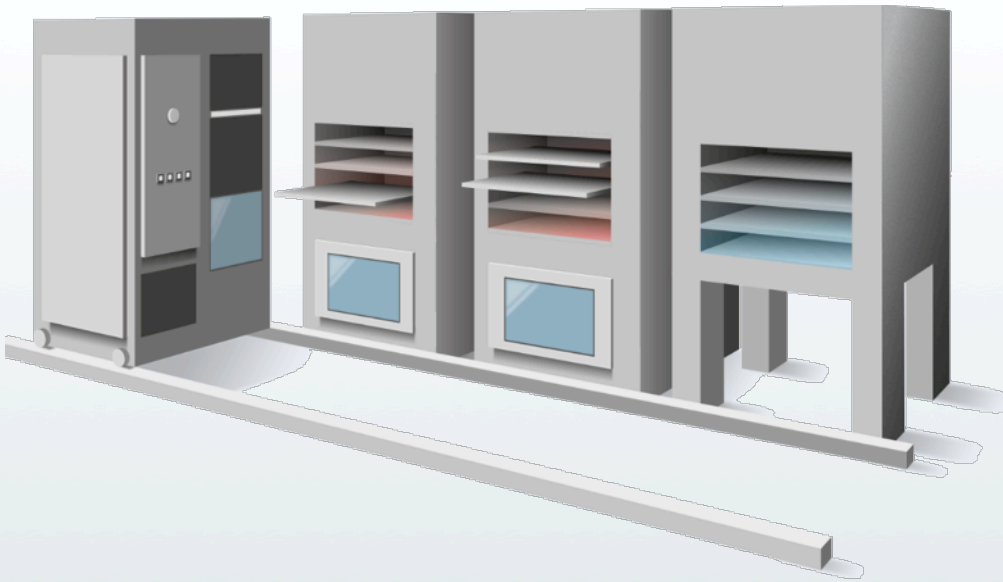


Inspection of the circuitry against digital ‘images’ (based upon data) to verify that it is free from such defects as shorts, opens, etc.

MANUFACTURING PROCESS

#6 – Lamination

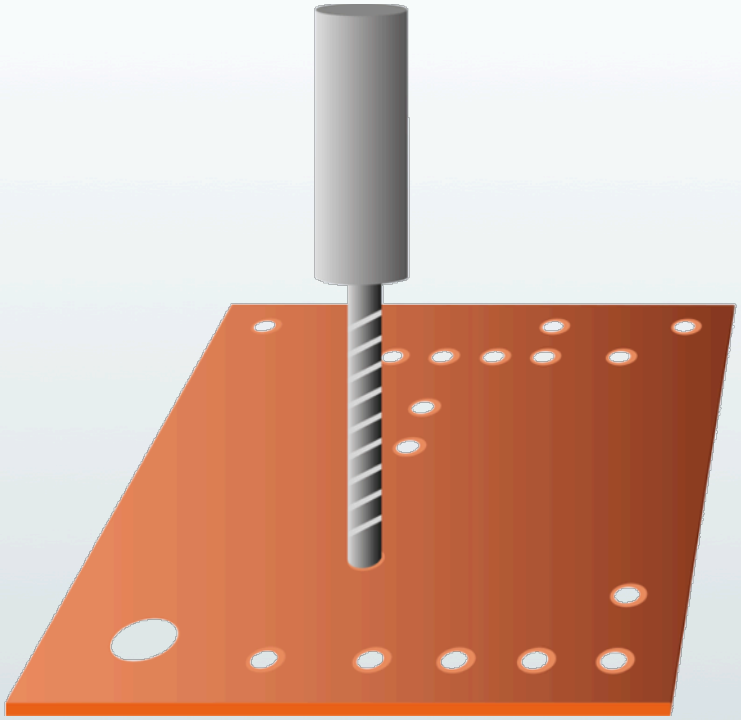




‘Fix’ the imaged inner layer cores and pre-preg, through bonding them together at a specific temperature and pressure for a specific time to form a solid, rigid stack up.

MANUFACTURING PROCESS

#7 – Drilling



Mechanical drilling of holes to facilitate the provision of electrical continuity between layers.
At this moment, the barrel of the hole has NO metallic deposit.

MANUFACTURING PROCESS

Electroless and Panel plating

Using the two processes the aim is to provide a uniform deposit of copper onto the hole wall through both chemical and electrochemical reactions.

Electroless copper is there only to provide a very thin deposit of ≤ 1um that covers the hole wall and also the complete panel.

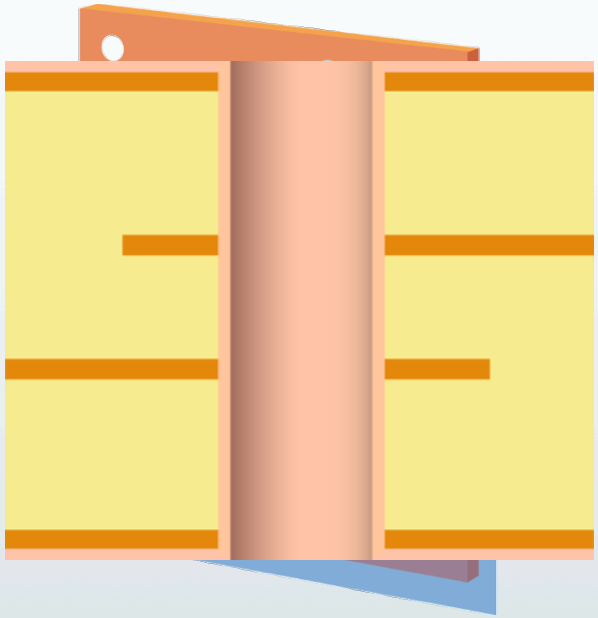
A complex chemical process that utilises a log of chemistry and with this being the base deposit, if this is poorly controlled then reliability is compromised.

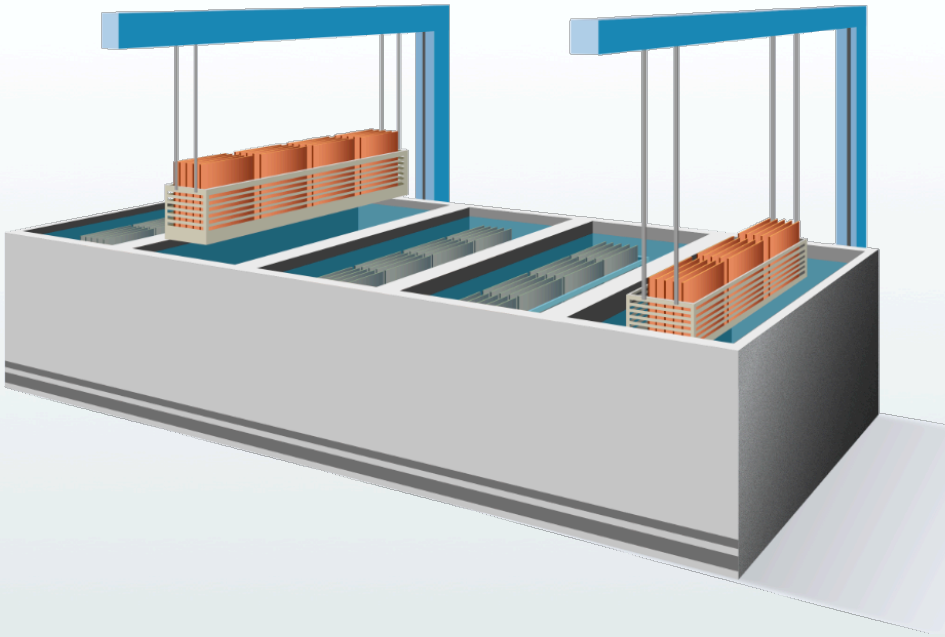
Panel plating follows on from electroless to provide a thicker deposit of copper on top of the electroless deposit – typically 5 to 8 um.

The combination is used to optimise the amount of copper that is to be plated and etched in order to achieve the track and gap demands.

MANUFACTURING PROCESS

#8 – PTH / Electroless

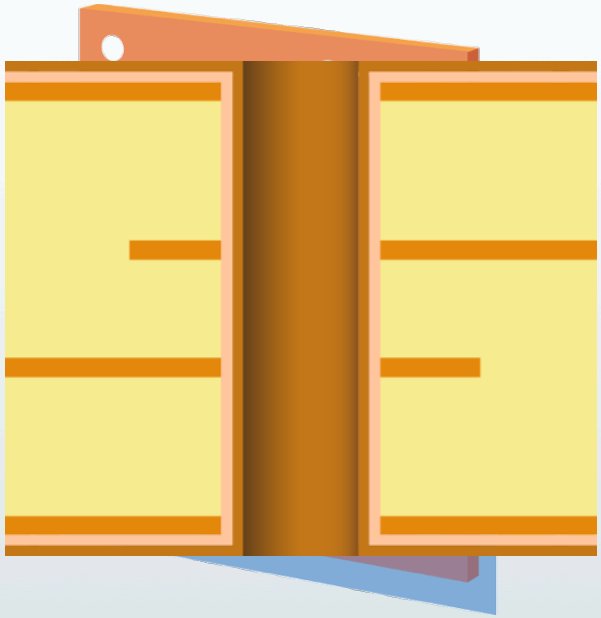


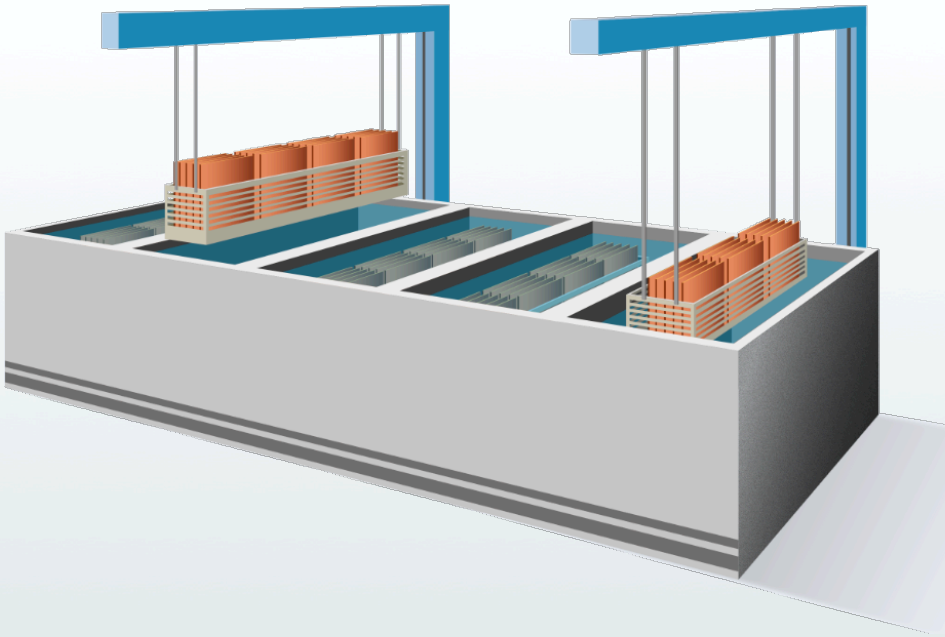


PTH provides a very thin deposit (<1um) over all surface – on the outer surface and within the barrel of the hole. A special process as it supports metallic plating onto non-metallic surfaces (inside the hole)

MANUFACTURING PROCESS

#9 – Panel plating



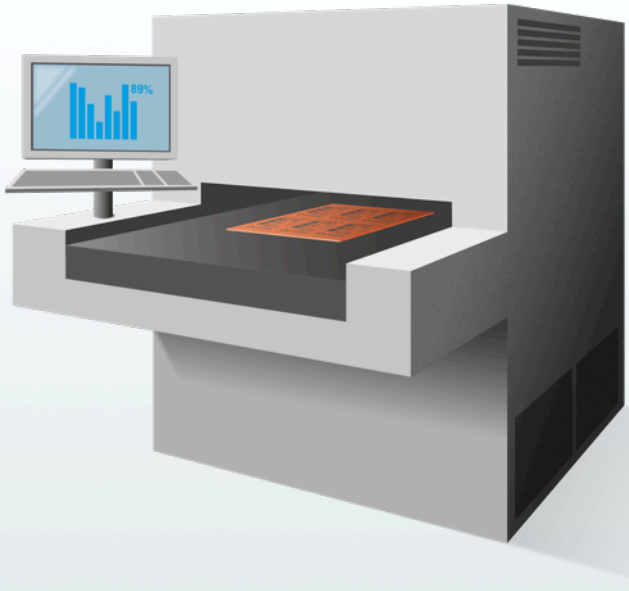


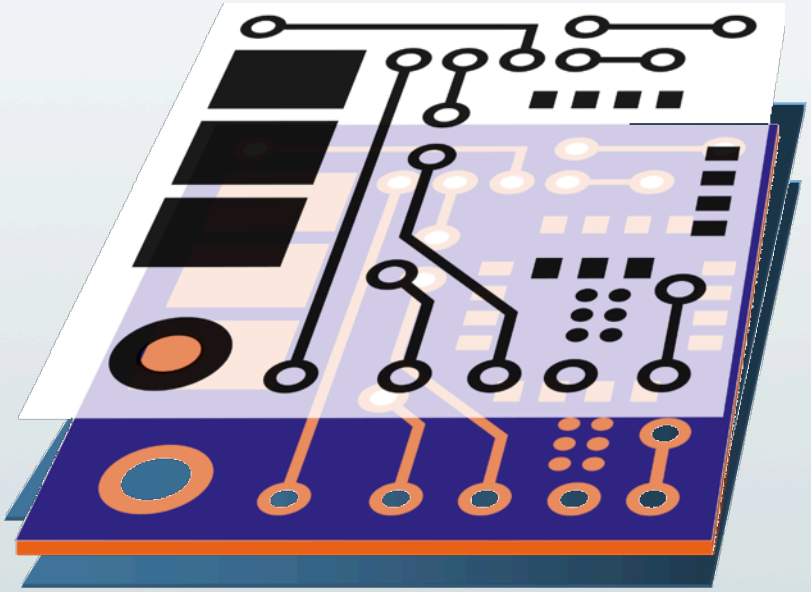
Adds a thicker deposit of copper (5 – 8um) onto the thin amount plated during PTH process. Provides the basis for a more reliable thickness of copper through the hole.

MANUFACTURING PROCESS

#10 – Outer layer image

Similar to inner layer, but with one difference - we remove dry film where we want to keep the copper / define circuitry.

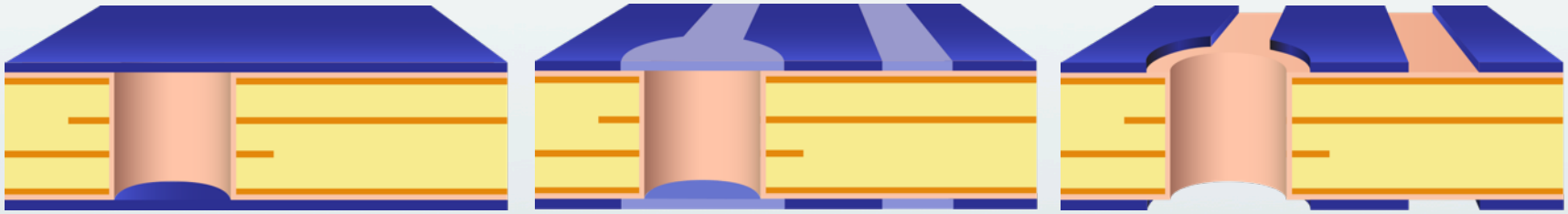




MANUFACTURING PROCESS

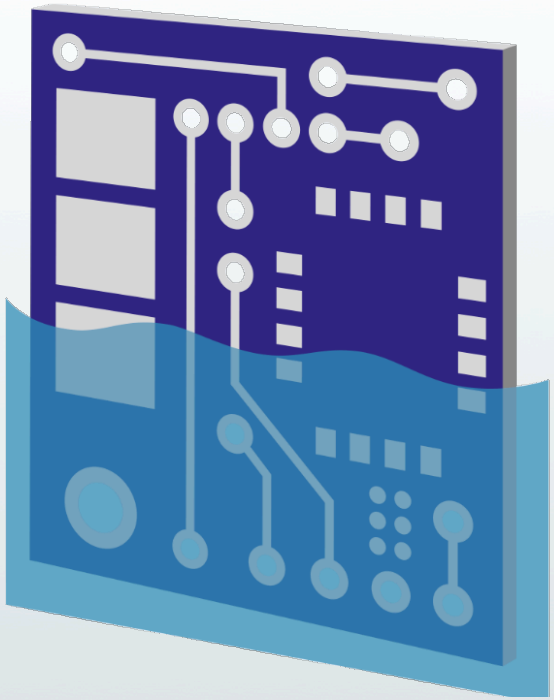
#10 – Outer layer image

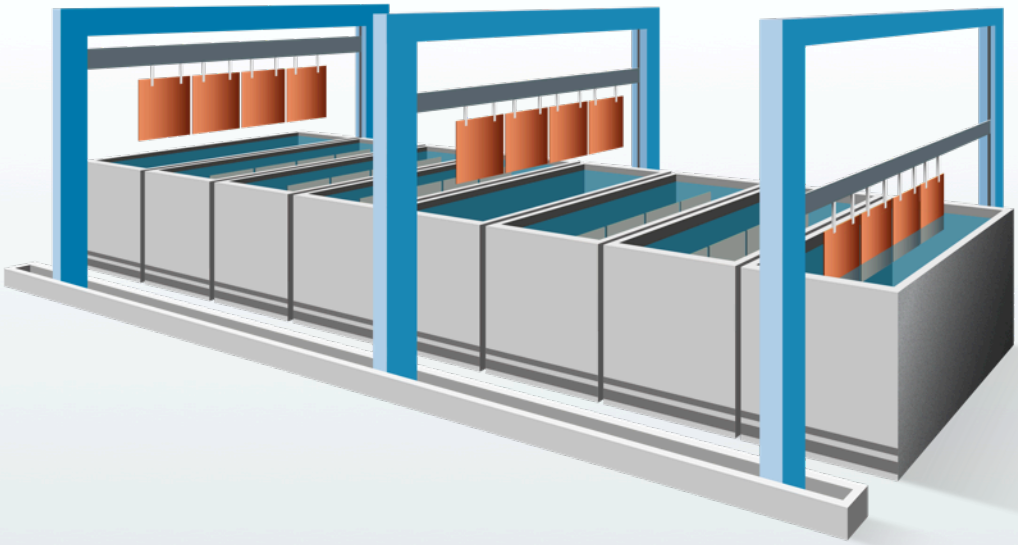
Dry film transitions – from application to imaging to developing.



MANUFACTURING PROCESS

#11 – Pattern plate



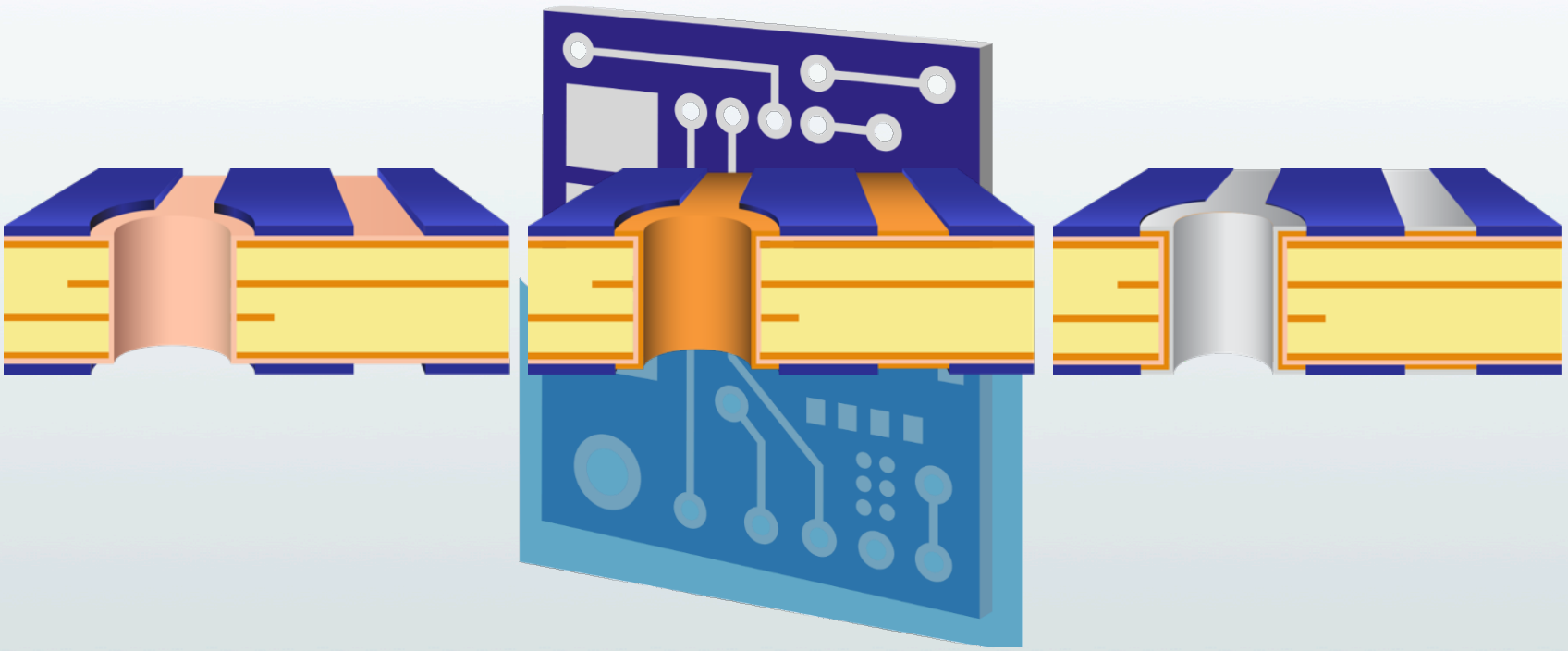


Additional plating deposited in areas exposed by imaging process. Finished plating thickness meets NCAB demands of 20um min, 25um average through the hole.

MANUFACTURING PROCESS

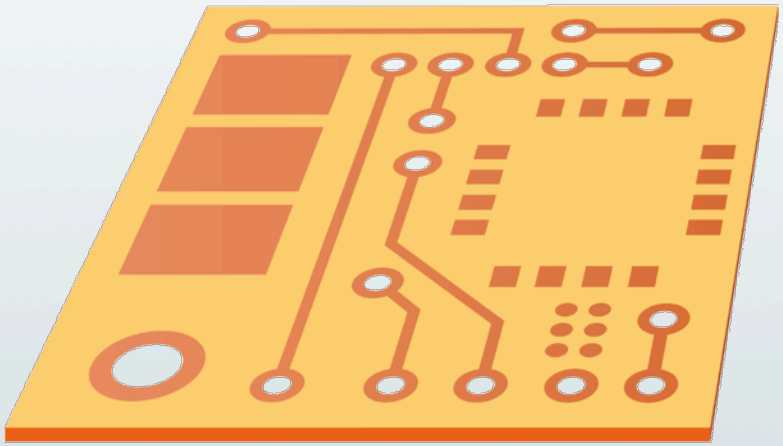
#11 – Pattern plate

Basic steps in pattern plate process.



MANUFACTURING PROCESS

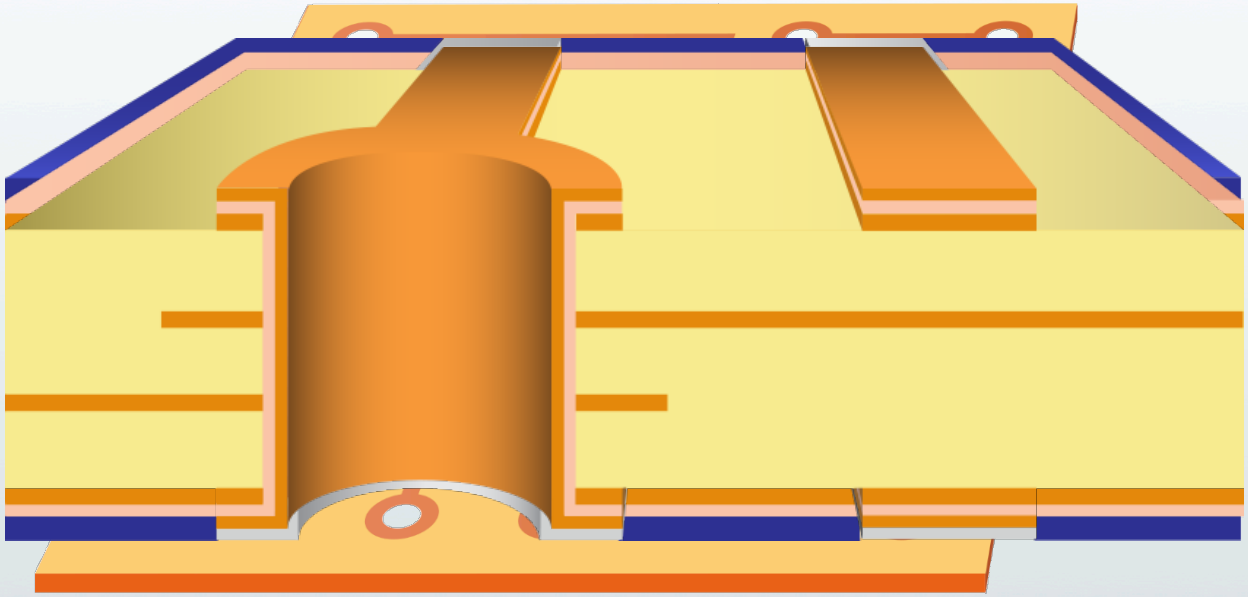
#12 – Outer layer etch



Removal of the remaining dry film (blue), etching of the unwanted & exposed copper and tin - leaving the copper (under the tin) that defines the circuitry.

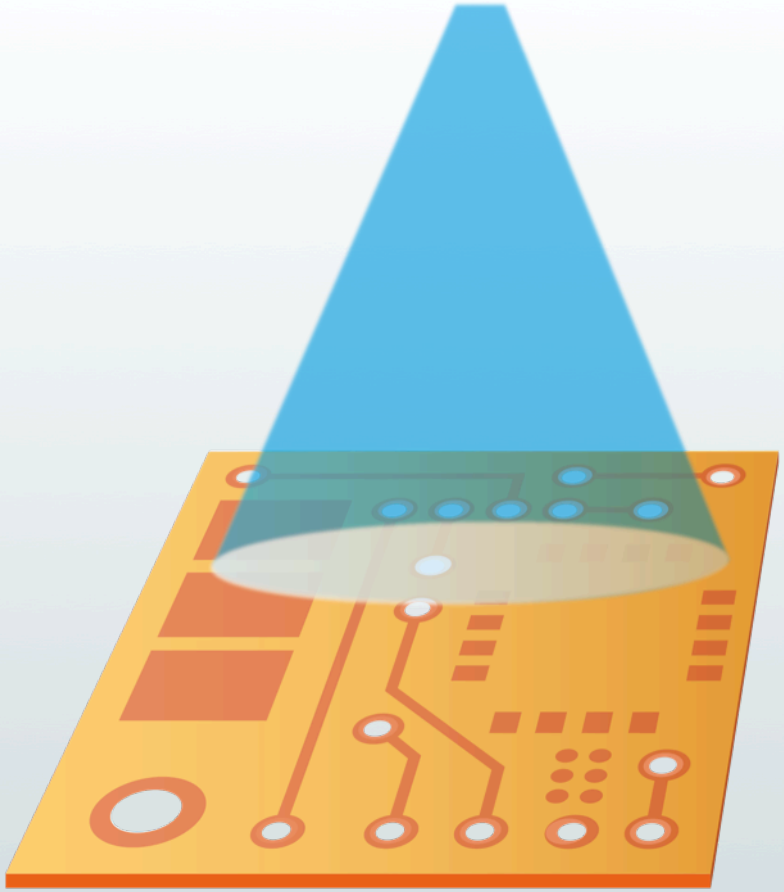
MANUFACTURING PROCESS

#12 – Outer layer etch



MANUFACTURING PROCESS

#13 – Outer layer AOI

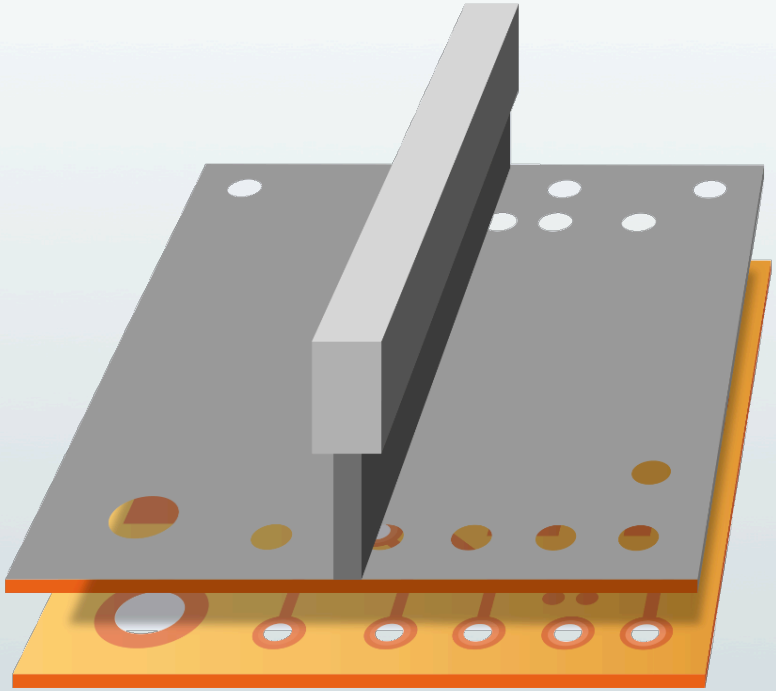


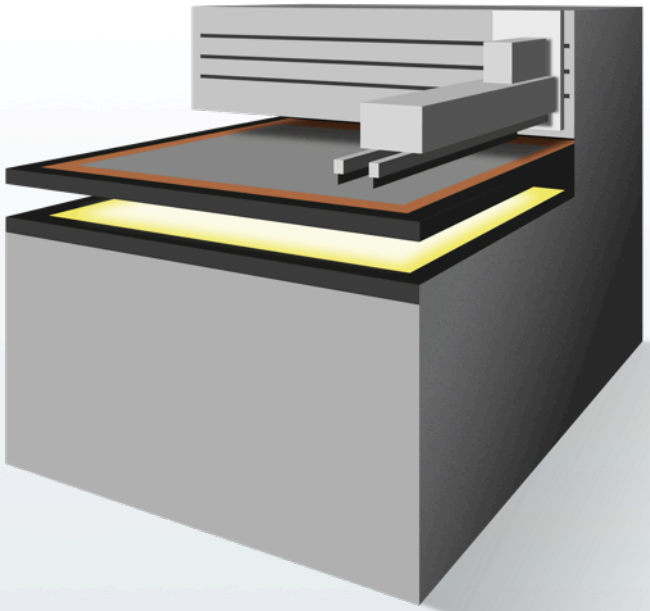
Inspection of the circuitry against digital ‘images’ (based upon data) to verify that it is free from such defects as shorts, opens, etc.

MANUFACTURING PROCESS

#14 – Via hole plugging

Screen printing to push soldermask into holes – a separate operation using an aluminium stencil

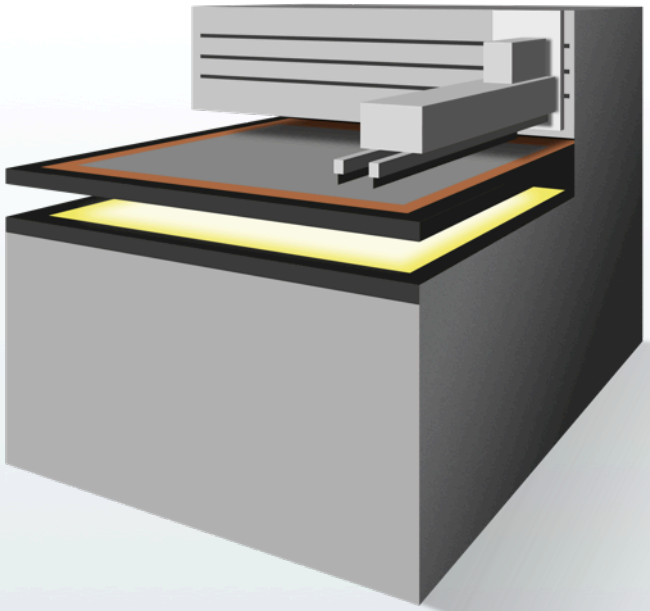


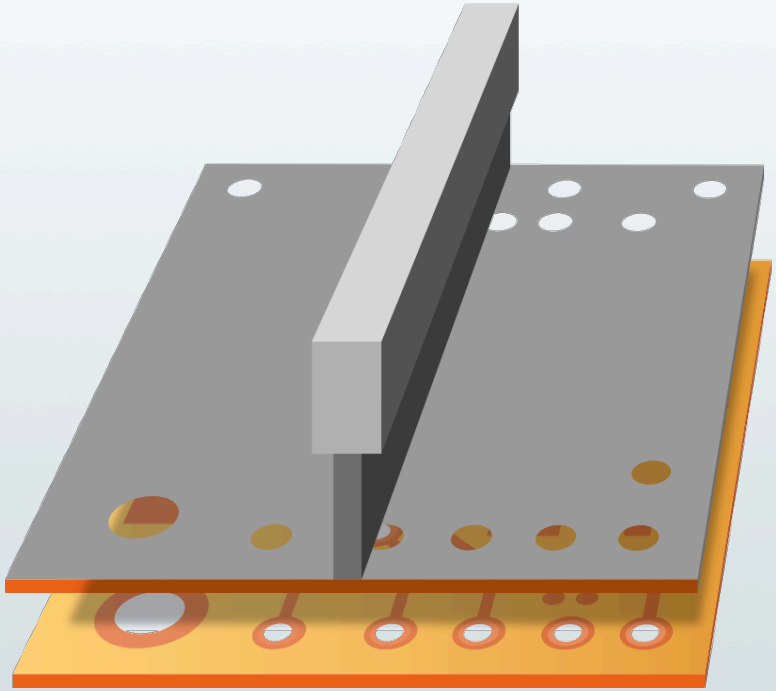


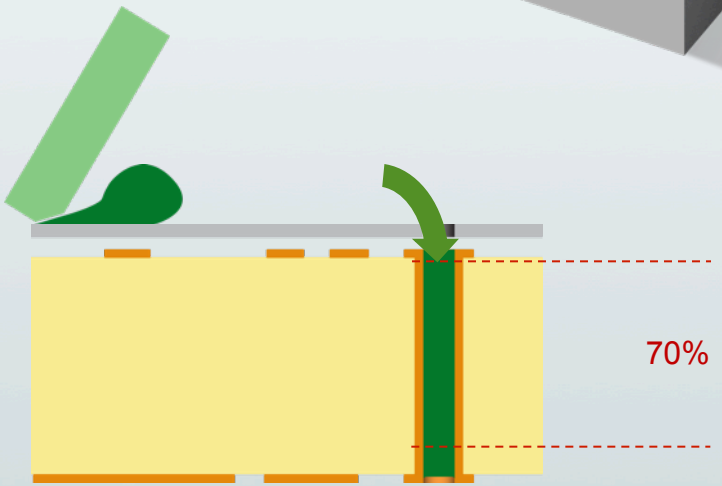
MANUFACTURING PROCESS

#14 – Via hole plugging

Screen printing to push soldermask into holes – a separate operation using an aluminium stencil



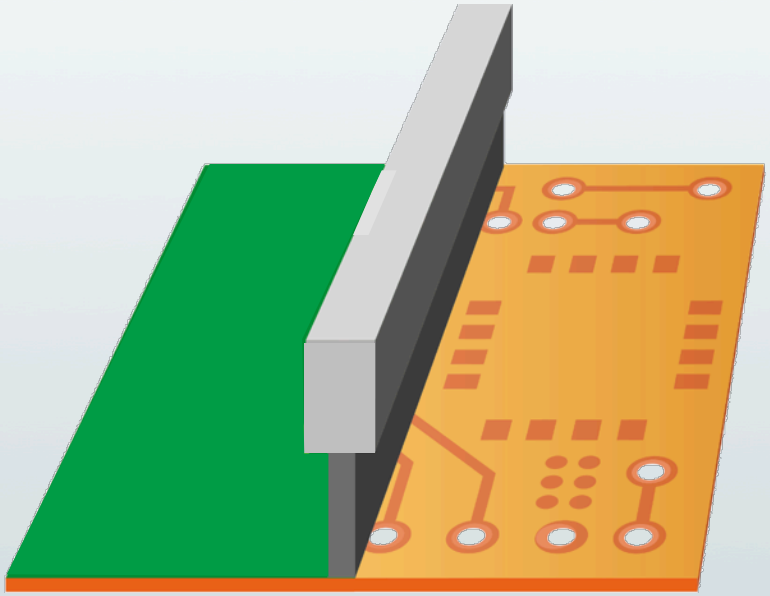




MANUFACTURING PROCESS

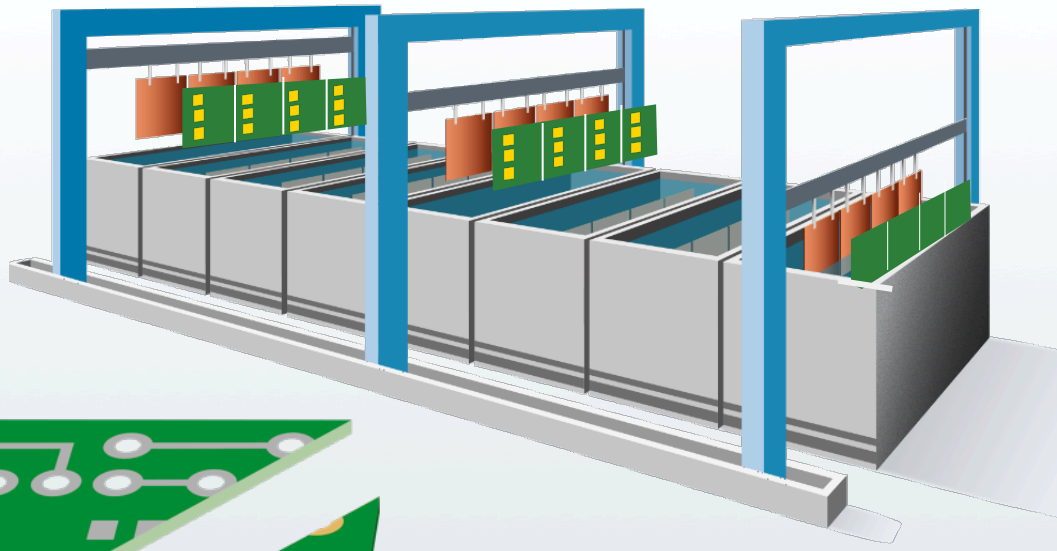
#15 – Soldermask

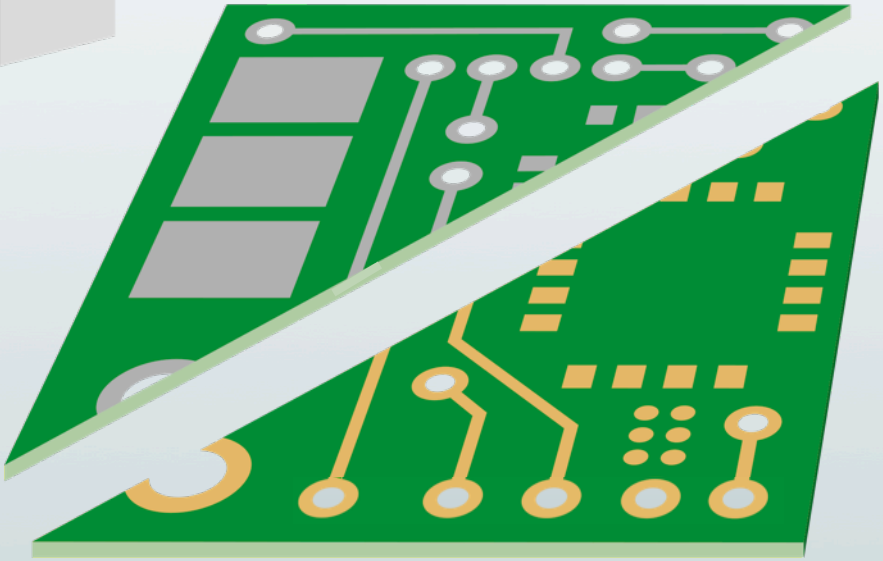
Soldermask is applied to the whole board. Exposed to UV (artworks again!) in areas we wish to keep, and then unexposed areas are washed / developed away.



MANUFACTURING PROCESS

#16 – Surface finishes

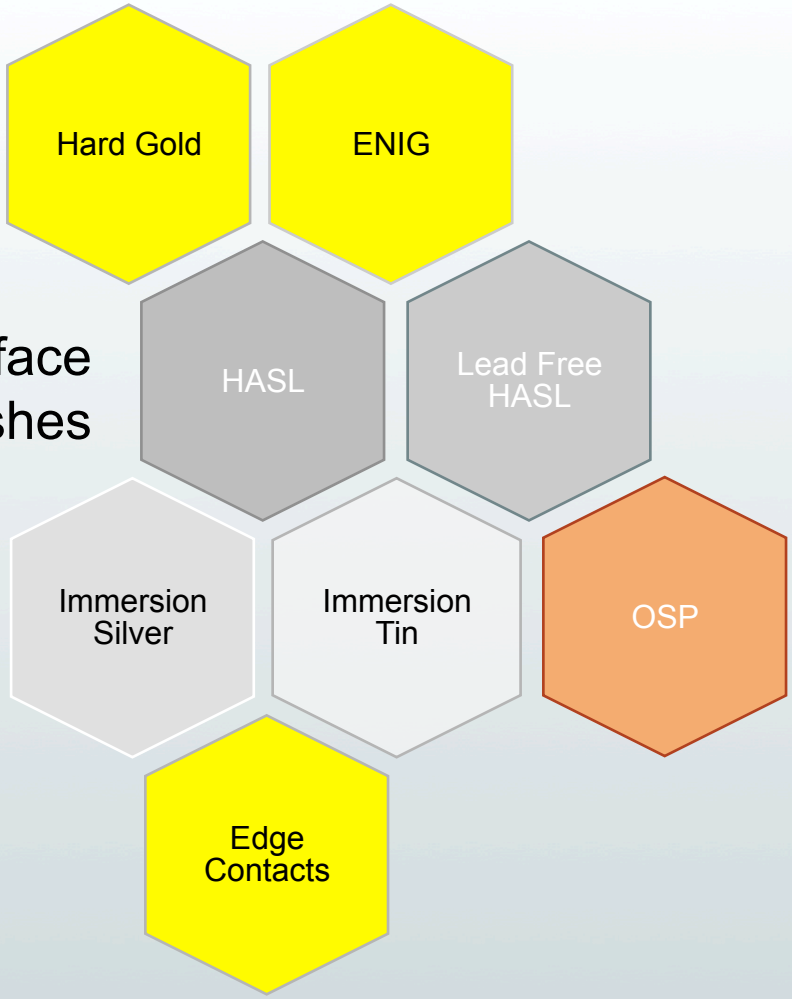




MANUFACTURING PROCESS

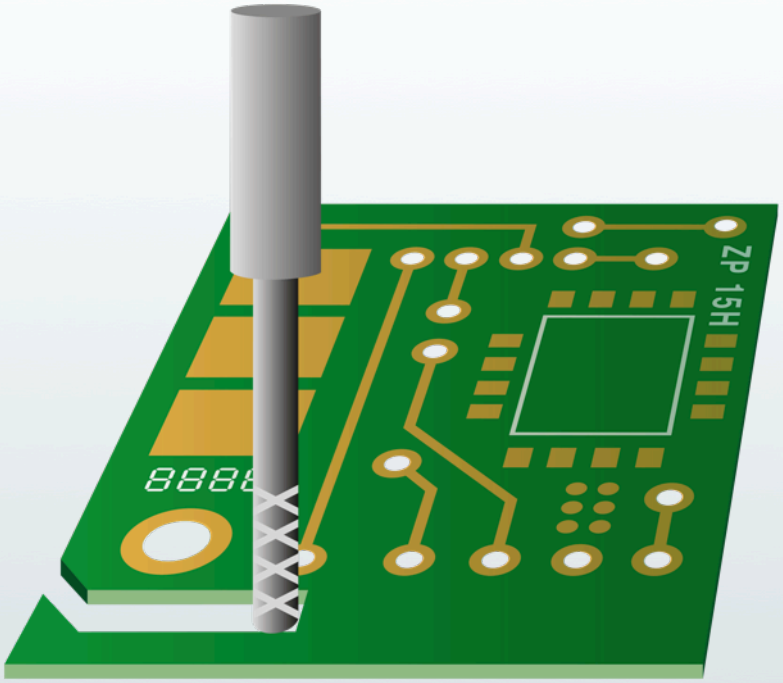
#16 – Surface finishes

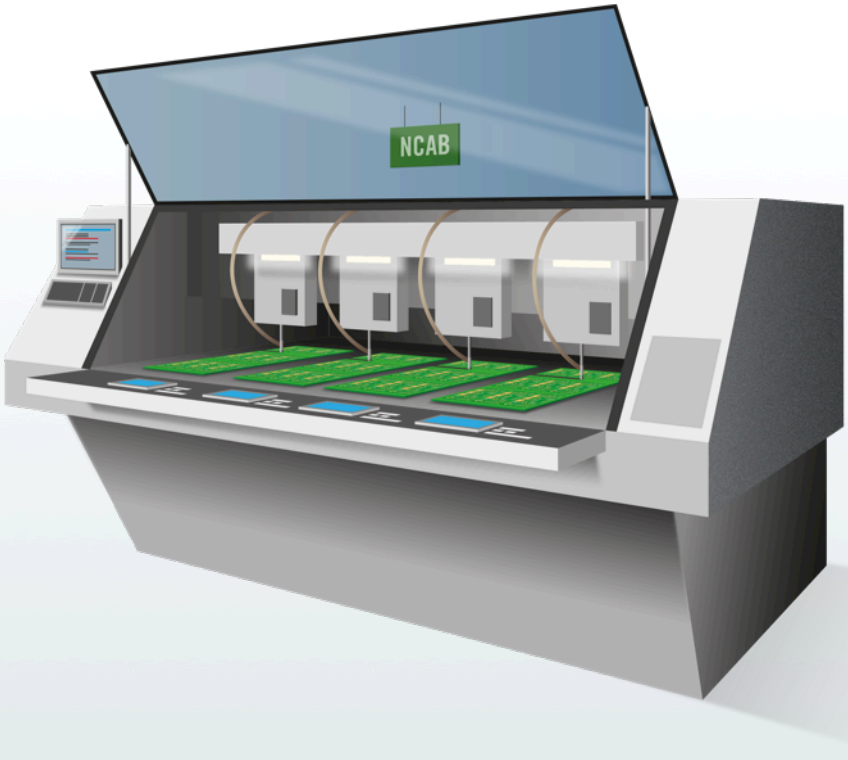
Commonly available surface finishes



MANUFACTURING PROCESS

#17 – Profile

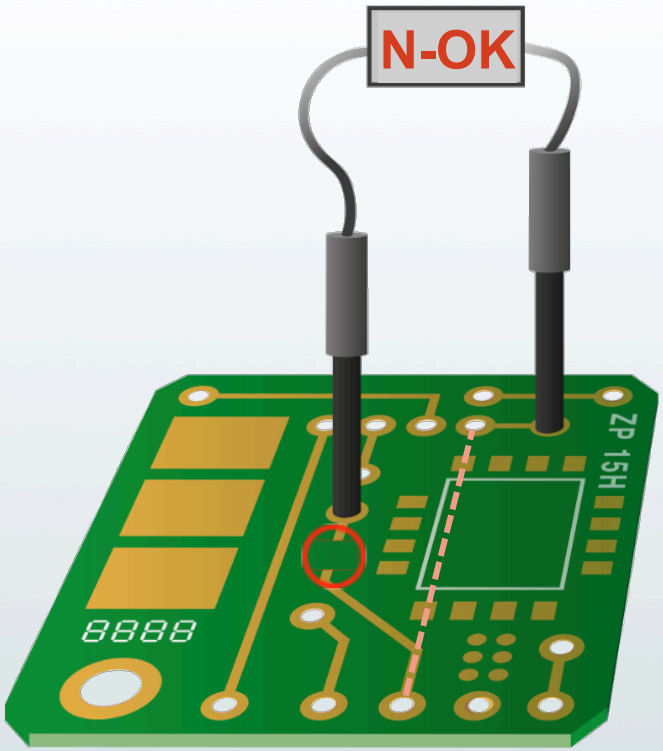


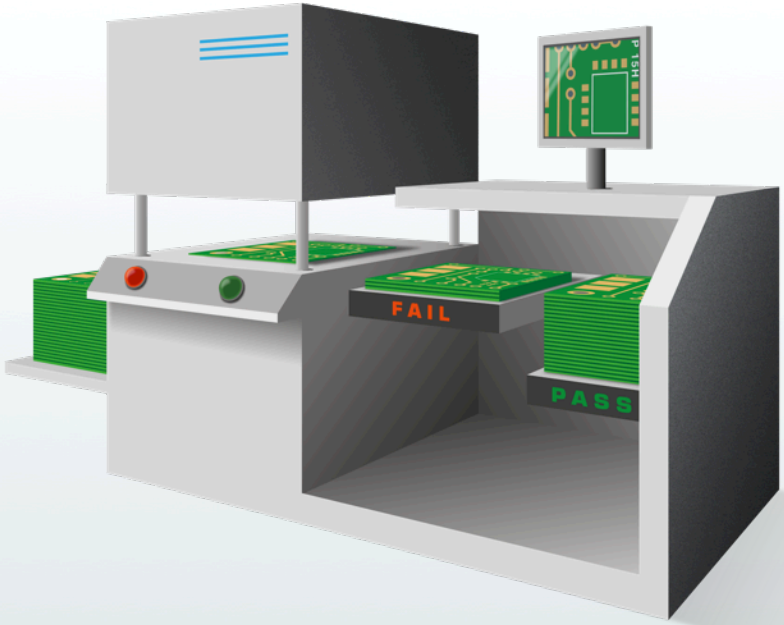


Machining the panels to provide circuits of a specific shape and size.

MANUFACTURING PROCESS

#18 – Electrical test





Used for checking the integrity of the tracks and the through hole interconnections – ensuring there are no open or short circuits.

MANUFACTURING PROCESS

#19 – Final Inspection

Visual checking of the PCB for cosmetic defects against NCAB demands and customer / IPC demands.

Using manual visual inspection and also AVI – compares digitally to identified anomalies at a speed faster than the human eye.

All orders are also subjected to a full inspection including dimensional, solderability, microsection, etc.